

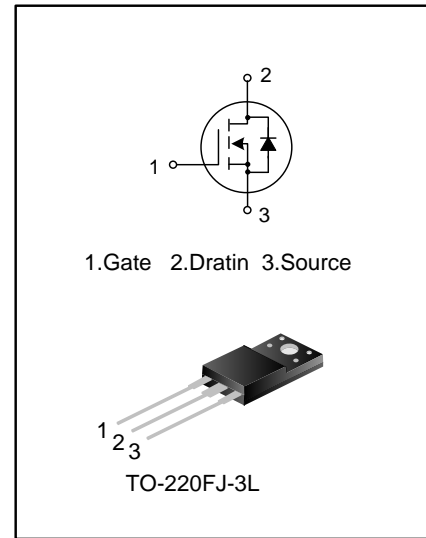
## 20A, 600V DP MOS POWER TRANSISTOR

### GENERAL DESCRIPTION

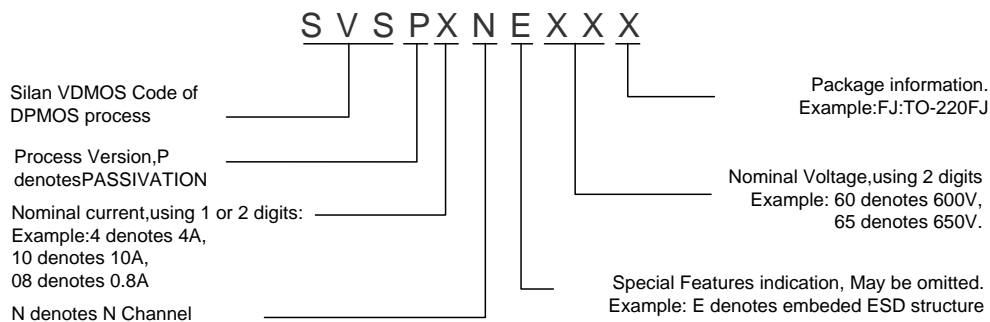
SVSP20N60FJ is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's DP MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, for example. it is suitable for hard and soft switching topologies.

### FEATURES

- ◆ 20A, 600V,  $R_{DS(on)}(typ.)=0.16\Omega@V_{GS}=10V$
- ◆ New revolutionary high voltage technology
- ◆ Ultra low gate charge
- ◆ Periodic avalanche rated
- ◆ Extreme dv/dt rated
- ◆ High peak current capability



### NOMENCLATURE



### ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVSP20N60FJ	TO-220FJ-3L	P20N60FJ	Halogen free	Tube

**ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C, unless otherwise noted)**

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V <sub>DS</sub>	600	V
Gate-Source Voltage		V <sub>GS</sub>	±30	V
Drain Current	T <sub>C</sub> =25°C	I <sub>D</sub>	20	A
	T <sub>C</sub> =100°C		12	
Drain Current Pulsed		I <sub>DM</sub>	80	A
Power Dissipation(T <sub>C</sub> =25°C)		P <sub>D</sub>	45	W
-Derate above 25°C			0.36	W/°C
Single Pulsed Avalanche Energy (Note 1)		E <sub>AS</sub>	854	mJ
Reverse diode dv/dt (Note 2)		dv/dt	15	V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	50	V/ns
Operation Junction Temperature Range		T <sub>J</sub>	-55~+150	°C
Storage Temperature Range		T <sub>stg</sub>	-55~+150	°C

**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	2.78	°C/W
Thermal Resistance, junction-to-Ambient	R <sub>θJA</sub>	62.5	°C/W

**ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C, unless otherwise noted)**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	600	--	--	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V	--	--	200	nA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	--	--	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	2.0	--	4.0	V
Static Drain-Source On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A				
		T <sub>J</sub> =25°C	--	0.16	0.19	Ω
		T <sub>J</sub> =125°C	--	0.30	--	
Gate resistance	R <sub>g</sub>	f=1.0MHz	--	1.7	--	Ω
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V, f=1.0MHz	--	1300	--	pF
Output Capacitance	C <sub>oss</sub>		--	88	--	
Reverse Transfer Capacitance	C <sub>rSS</sub>		--	2.67	--	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =300V, V <sub>GS</sub> =10V, R <sub>G</sub> =25Ω, I <sub>D</sub> =20A (Note 2,3)	--	18.53	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	51.03	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	101.6	--	
Turn-off Fall Time	t <sub>f</sub>		--	51.6	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> =480V, V <sub>GS</sub> =10V, I <sub>D</sub> =20A (Note 2,3)	--	38.9	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	9.04	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	18.02	--	

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I <sub>S</sub>	Integral Reverse P-N Junction	--	--	20	A
Pulsed Source Current	I <sub>SM</sub>	Diode in the MOSFET	--	--	80	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V	--	--	1.2	V
Reverse Recovery Time	T <sub>rr</sub>	V <sub>DD</sub> =50V, I <sub>F</sub> =20A,	--	400	--	ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt=100A/μs	--	6.2	--	μC

**Notes:**

- L=79mH, I<sub>AS</sub>=4.2A, V<sub>DD</sub>=100V, R<sub>G</sub>=25Ω, starting temperature T<sub>J</sub>=25°C;
- V<sub>DS</sub>=0~400V, I<sub>SD</sub>≤20A, T<sub>J</sub>=25°C;
- V<sub>DS</sub>=0~480V;
- Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
- Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics

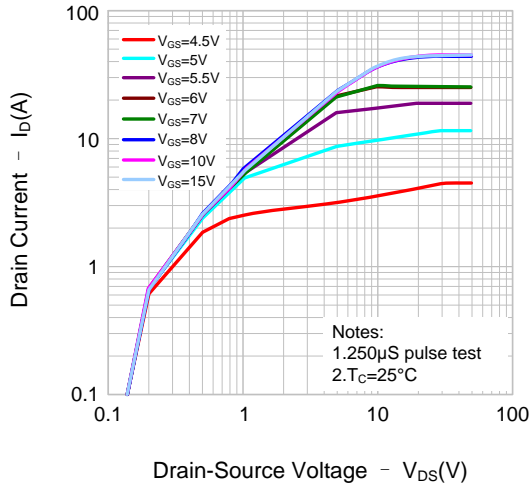


Figure 2. Transfer Characteristics

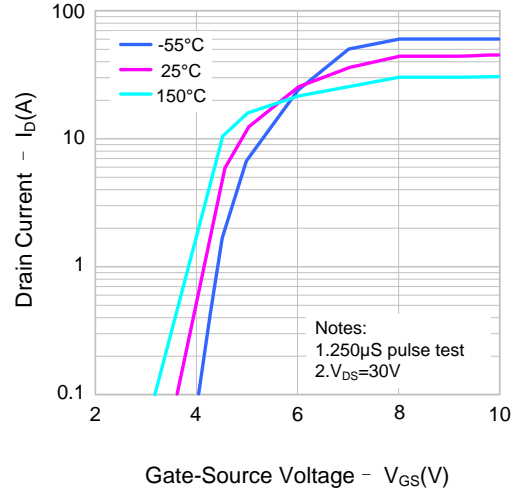


Figure 3. On-Resistance Variation vs. Drain Current

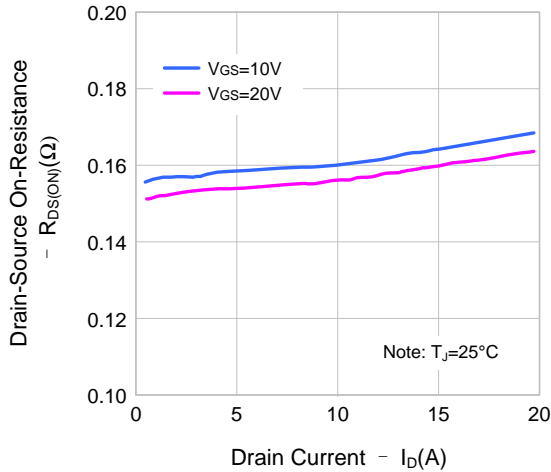


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

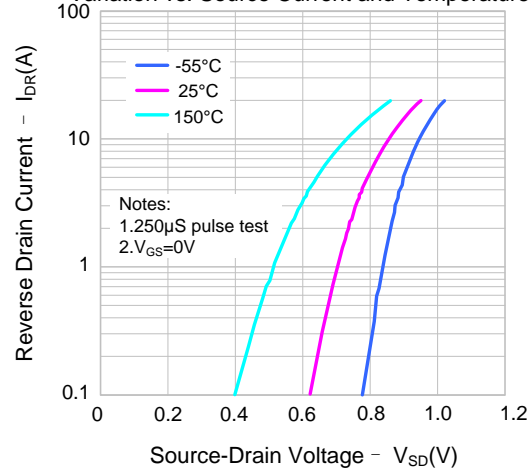


Figure 5. Capacitance Characteristics

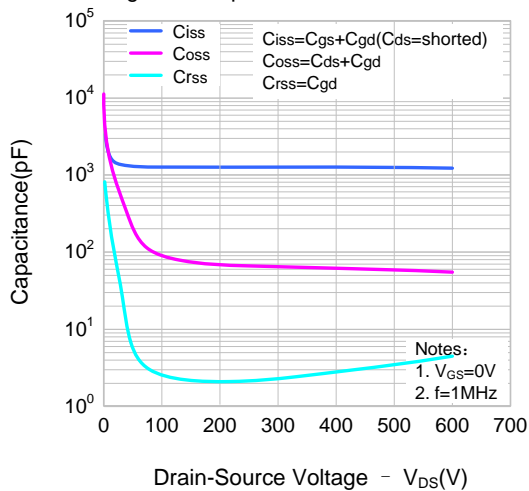
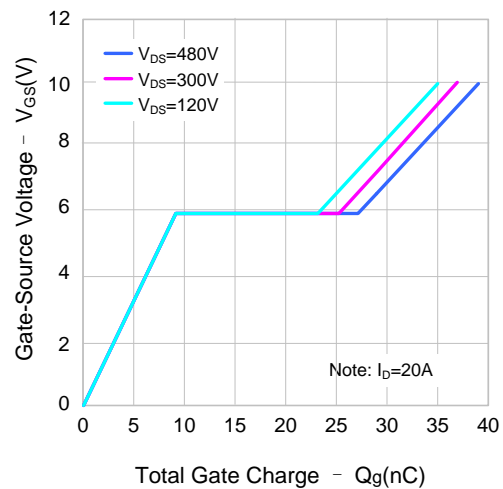


Figure 6. Gate Charge Characteristics



**TYPICAL CHARACTERISTICS(continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

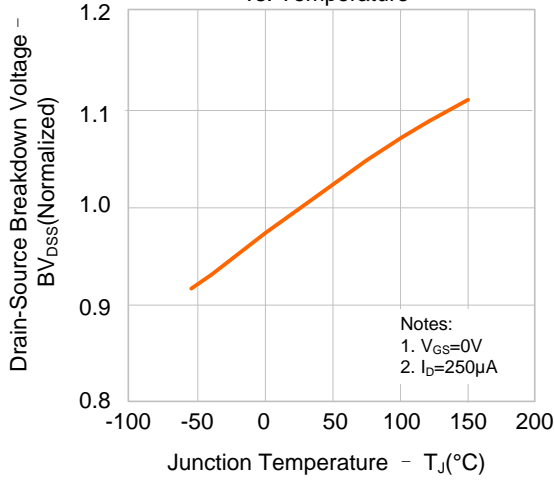


Figure 8. On-resistance Variation vs. Temperature

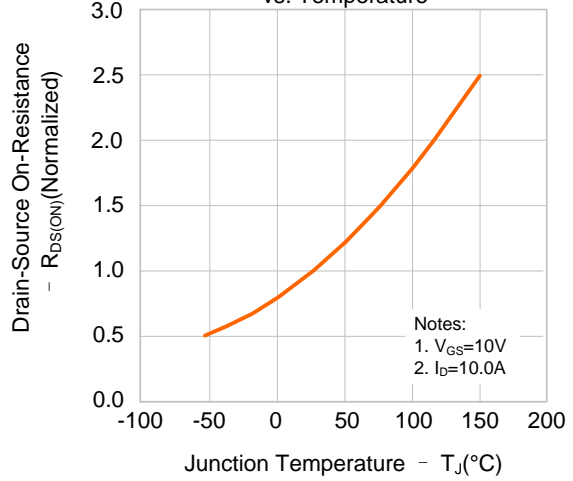
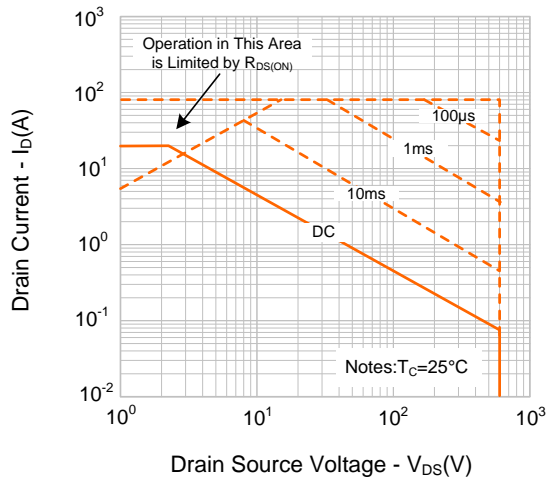
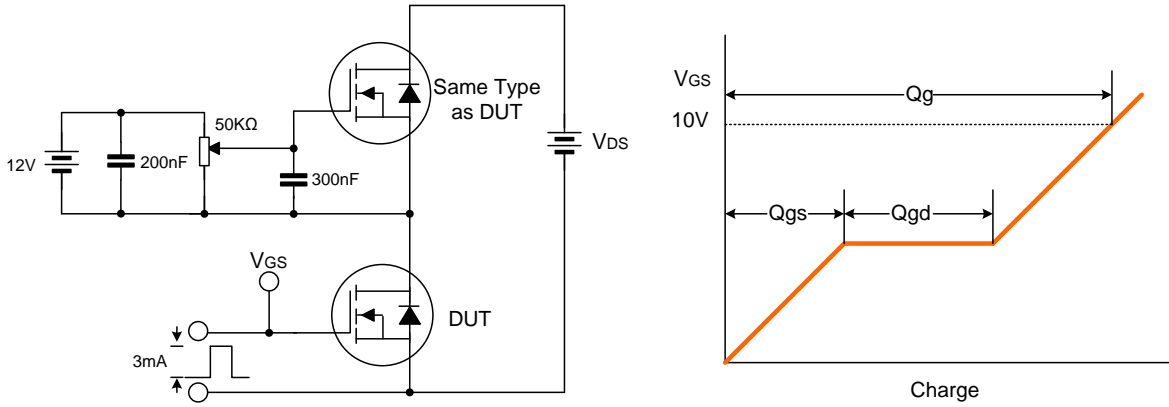


Figure 9. Max. Safe Operating Area

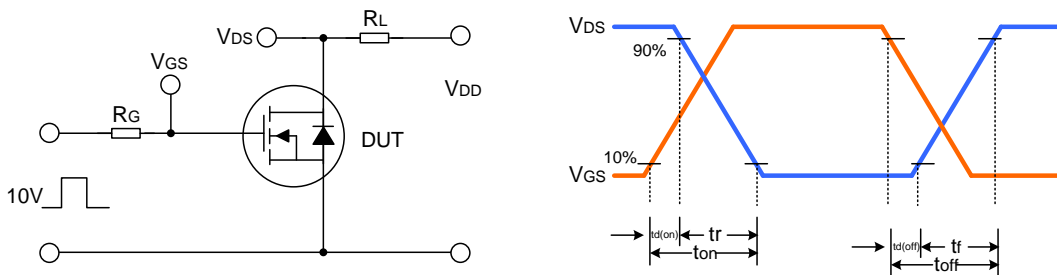


**TYPICAL TEST CIRCUIT**

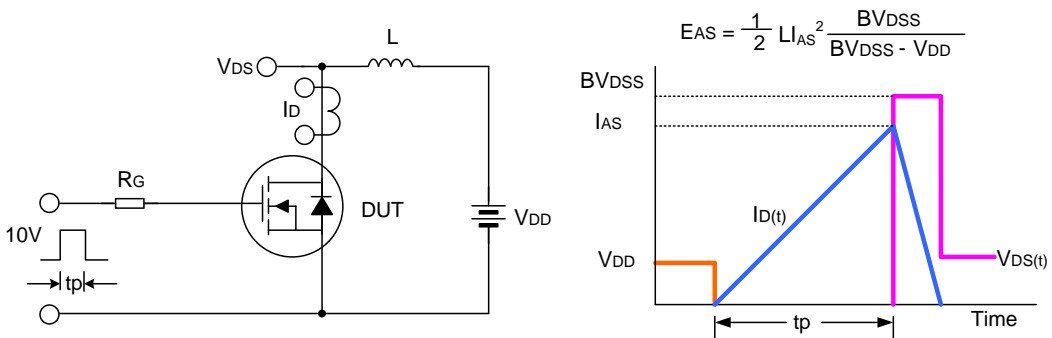
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



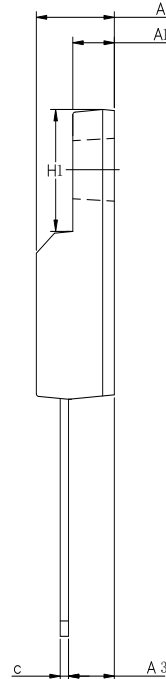
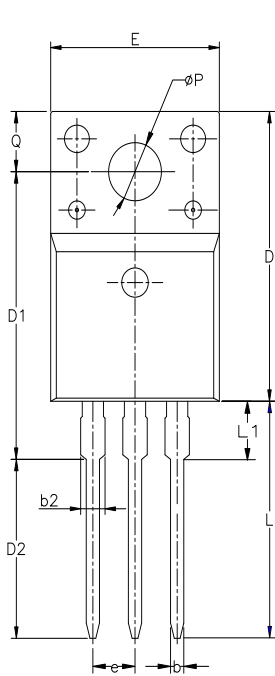
Unclamped Inductive Switching Test Circuit & Waveform



**PACKAGE OUTLINE**

**TO-220FJ-3L**

**UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
$\phi P$	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Rev.: 1.3

Revision History:

1. Update Fig 5
  2. Add dv/dt
- 

Rev.: 1.2

Revision History:

1. Modify values of  $I_{DSS}$  and  $V_{SD}$
- 

Rev.: 1.1

Revision History:

1. Modify Coss to 88 pf
  2. Update Figure 5
- 

Rev.: 1.0

Revision History:

1. First release
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