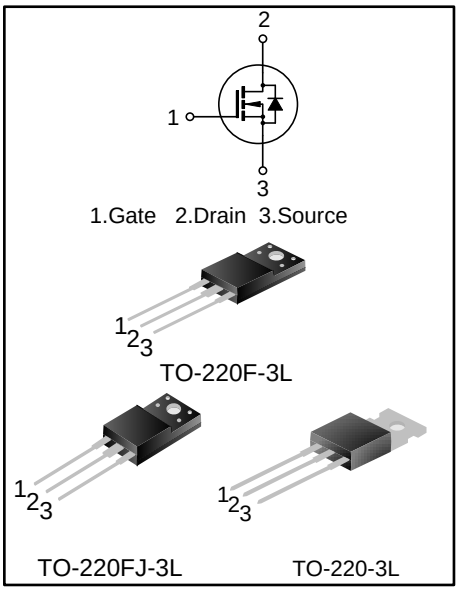
14A, 600V SUPER JUNCTION MOS POWER TRANSISTOR

DESCRIPTION

SVS14N60F(FJ)(T)D2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's super junction MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.



FEATURES

- 14A,600V, $R_{DS(on)(typ.)}$=0.25Ω@V_{GS}=10V
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVS14N60TD2	TO-220-3L	14N60TD2	Halogen free	Tube
SVS14N60FJD2	TO-220FJ-3L	14N60FJD2	Halogen free	Tube
SVS14N60FD2	TO-220F-3L	14N60FD2	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics		Symbol	Ratings		Unit
			SVS14N60TD2	SVS14N60F/FJD2	
Drain-Source Voltage		V_{DS}	600		V
Gate-Source Voltage		V_{GS}	±30		V
Drain Current	T_C=25°C	I_D	14		A
	T_C=100°C		8.8		
Drain Current Pulsed		I_{DM}	56		A
Power Dissipation (T_C=25°C)		P_D	120	38	W
- Derate above 25°C			0.96	0.3	W/°C
Single Pulsed Avalanche Energy (Note1)		E_{AS}	580		mJ
Reverse diode dv/dt	(Note 2)	dv/dt	15		V/ns
MOSFET dv/dt ruggedness	(Note 3)	dv/dt	50		V/ns
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value		Unit
		SVS14N60TD2	SVS14N60F/FJD2	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.04	3.29	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA		600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V		--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V		--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA		2.0	--	4.0	V
Static Drain- Source on State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=7.0A	Tj=25°C	--	0.25	0.28	Ω
			Tj=125°C	--	0.51	--	
Gate resistance	R_g	f=1.0MHz		--	3.15	--	Ω
Input Capacitance	C_{iss}	f=1MHz, V_{GS}=0V, V_{DS}=100V		--	838	--	pF
Output Capacitance	C_{oss}			--	48	--	
Reverse Transfer Capacitance	C_{rss}			--	2.9	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V, V_{GS}=10V, R_G=24Ω, I_D=14A (Note 4,5)		--	15	--	ns
Turn-on Rise Time	t_r			--	48	--	
Turn-off Delay Time	$t_{d(off)}$			--	68	--	
Turn-off Fall Time	t_f			--	33	--	
Total Gate Charge	Q_g	V_{DD}=480V, V_{GS}=10V, I_D=14A (Note 4,5)		--	28	--	nC
Gate-Source Charge	Q_{gs}			--	6.6	--	
Gate-Drain Charge	Q_{gd}			--	14	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	14	A
Pulsed Source Current	I_{SM}		--	--	56	
Diode Forward Voltage	V_{SD}	I_S=14A, V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	V_{DD}=50V, I_F=14A , dI_F/dt=100A/μs (Note 2)	--	404	--	ns
Reverse Recovery Charge	Q_{rr}		--	4.9	--	μC

Notes:

1. L=79mH, I_{AS}=3.5A, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V, I_{SD}<=14A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

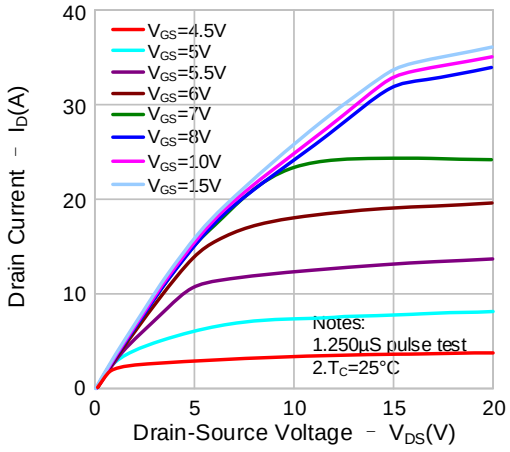


Figure 2. Transfer Characteristics

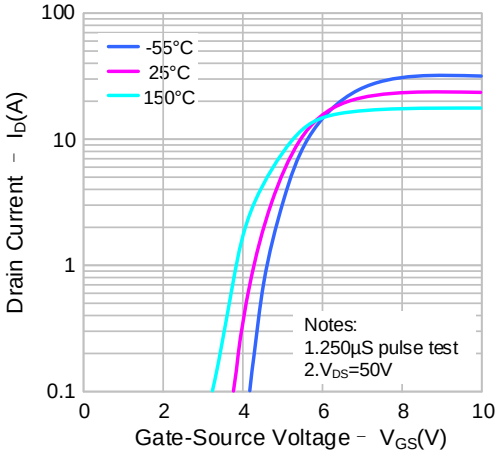


Figure 3. On-Resistance Variation vs. Drain Current

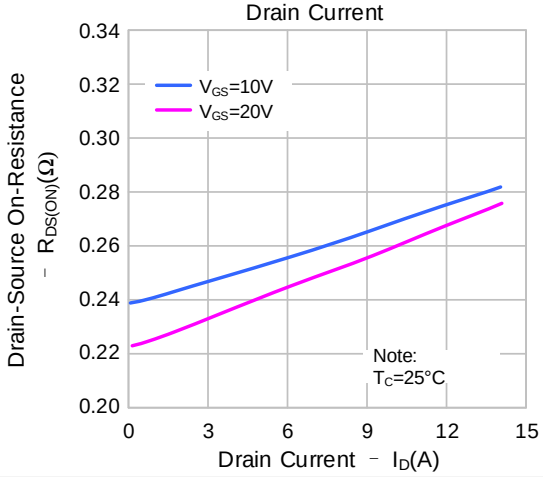


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

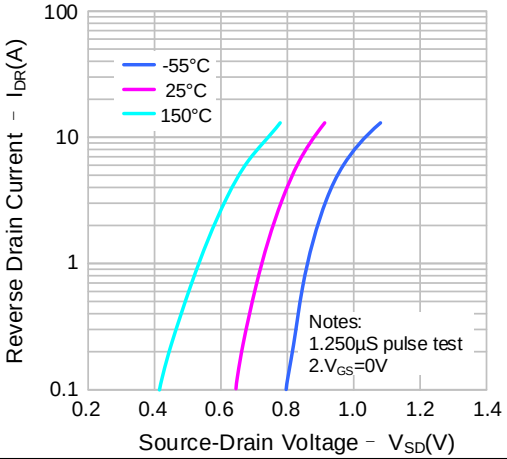


Figure 5. Capacitance Characteristics

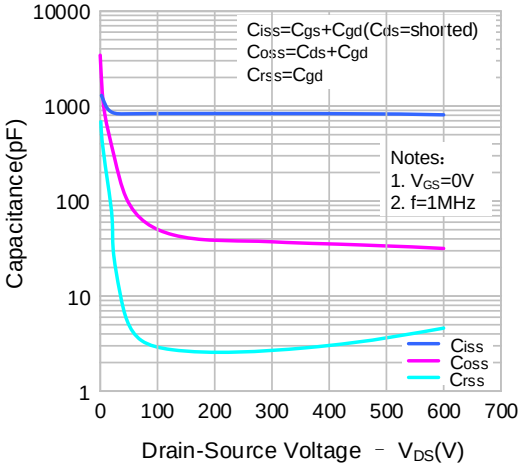
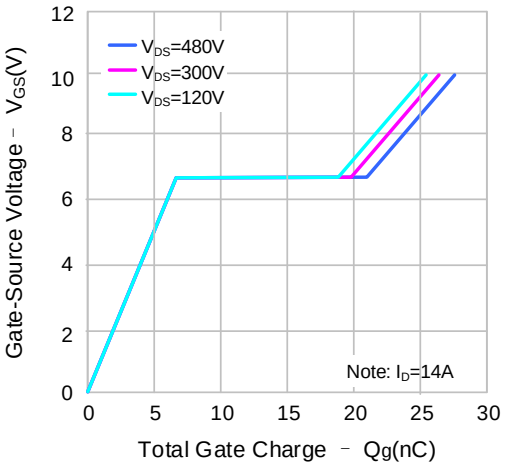


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

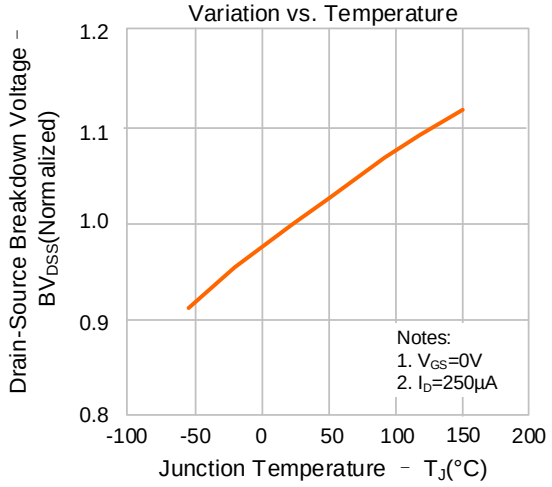


Figure 8. On-resistance Variation vs. Temperature

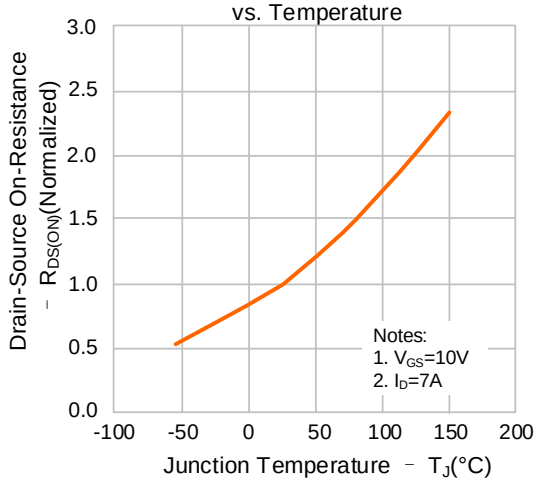


Figure 9-1. Max. Safe Operating Area(SVS14N60TD2)

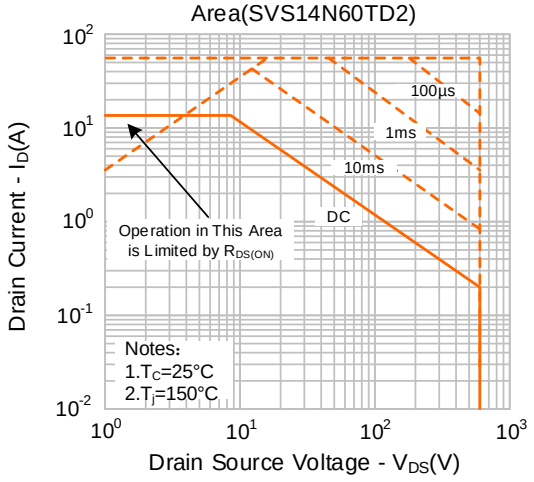
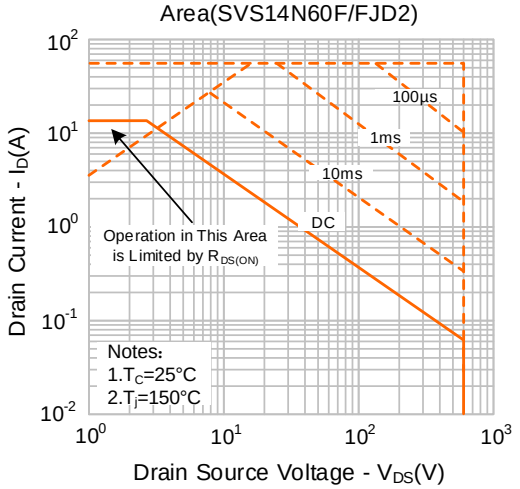
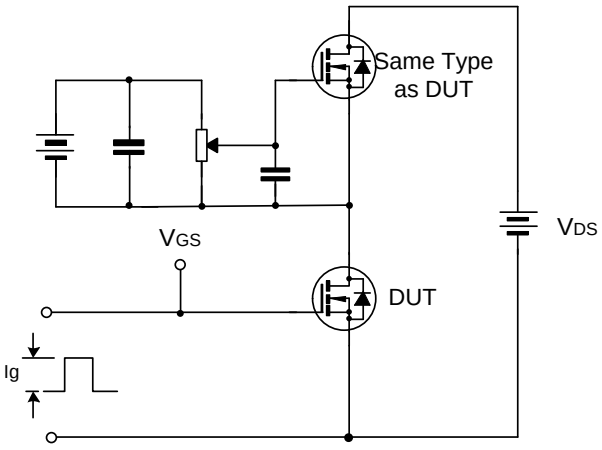


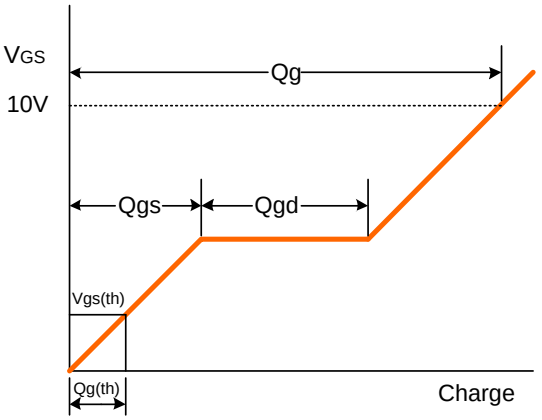
Figure 9-2. Max. Safe Operating Area(SVS14N60F/FJD2)



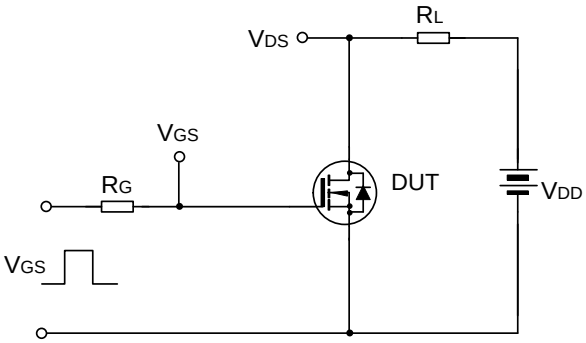
TYPICAL TEST CIRCUIT

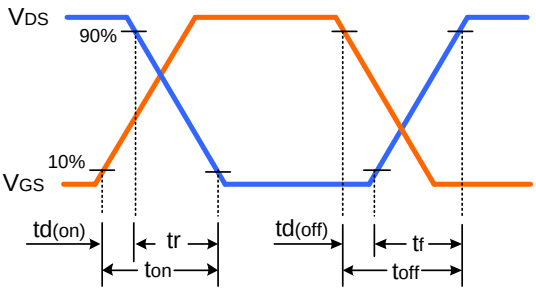
Gate Charge Test Circuit & Waveform



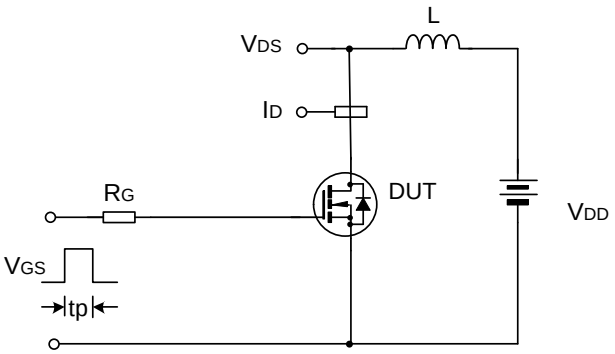


Resistive Switching Test Circuit & Waveform

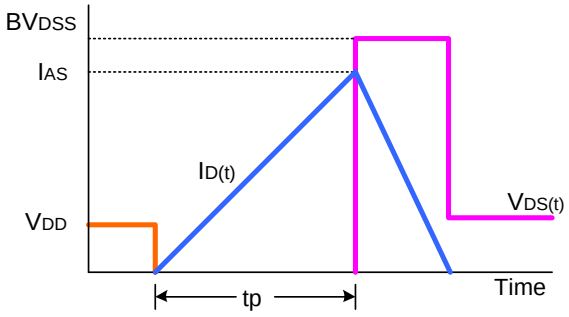




Unclamped Inductive Switching Test Circuit & Waveform

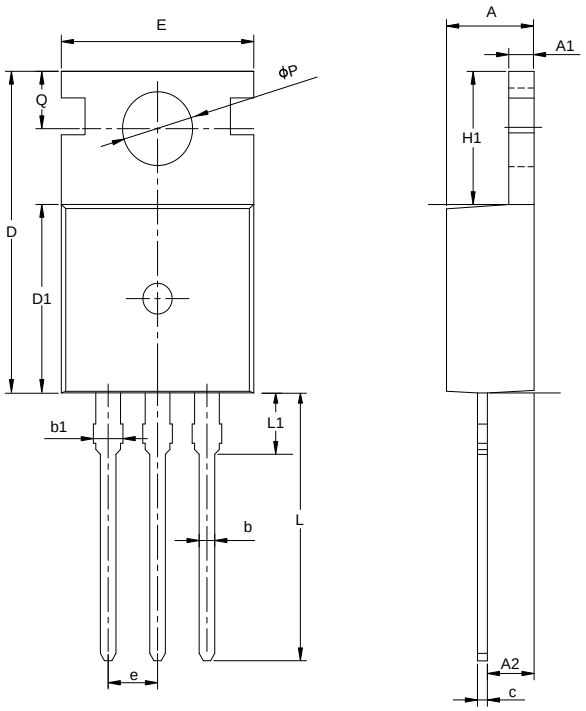


$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



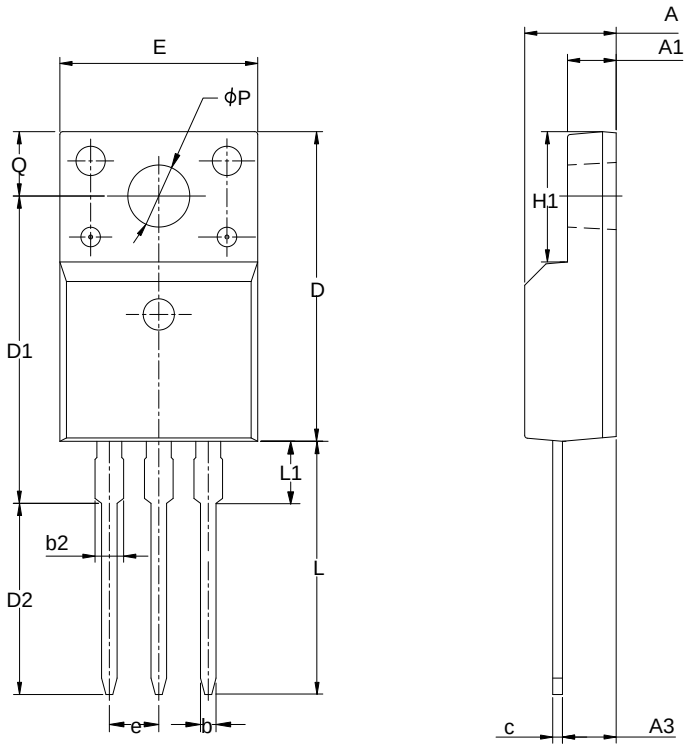
PACKAGE OUTLINE

TO-220-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

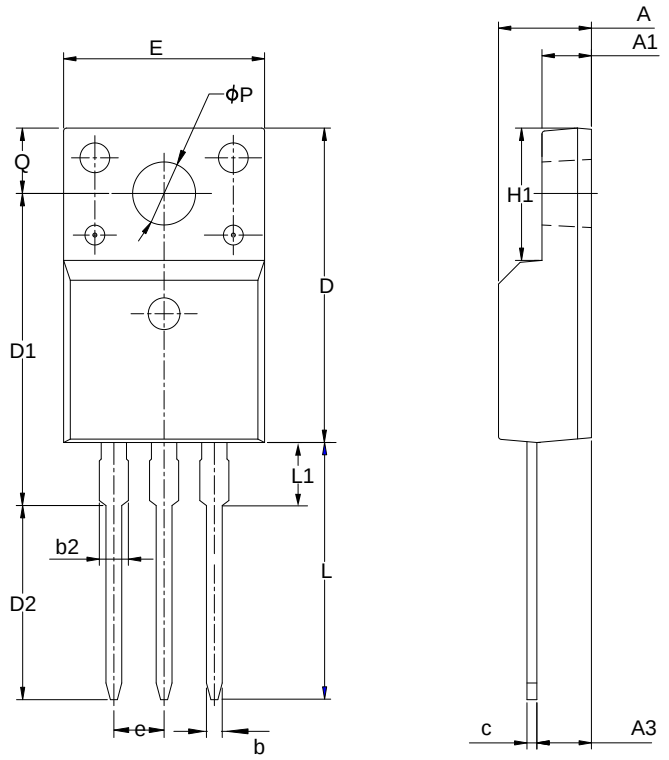
TO-220FJ-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

PACKAGE OUTLINE(CONTINUED)

TO-220F-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	–	–	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	–	–	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

Important notice :

1. **The instructions are subject to change without notice!**
2. **Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current. Please read the instructions carefully before using our products, including the circuit operation precautions.**
3. **Our products are consumer electronic products or the other civil electronic products.**
4. **When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.**
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Rev.: 1.5

Revision History:

1. Update electrical Diagram and typical test circuit
2. Update Curve template
3. Update package outline
4. Update important notice

Rev.: 1.4

Revision History:

1. Update Electrical characteristics
2. Modify Fig 5,6

Rev.: 1.3

Revision History:

1. Add TO-220F-3L
2. Add dv/dt
3. Modify Fig 2,5,6

Rev.: 1.2

Revision History:

1. Delete TO-252-2L
2. Modify the package outline of TO-220-3L

Rev.: 1.1

Revision History:

1. Add TO-252-2L
2. Modify characteristics and Fig5 and Fig6

Rev.: 1.0

Revision History:

1. First release