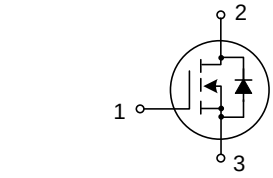
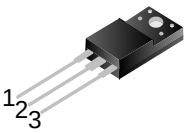
11A, 600V DP MOS POWER TRANSISTOR

DESCRIPTION

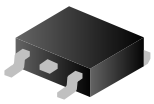
SVSP11N60FJ(D)D2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's DPMOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.



1.Gate 2.Drain 3.Source



TO-220FJ-3L



TO-252-2L

FEATURES

- 11A,600V, $R_{DS(on)(typ.)}$=0.3Ω@V_{GS}=10V
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVSP11N60FJD2	TO-220FJ-3L	P11N60FJD2	Halogen free	Tube
SVSP11N60DD2TR	TO-252-2L	P11N60D	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, T_C=25°C)

Characteristics		Symbol	Ratings		Unit
			SVSP11N60FJD2	SVSP11N60DD2	
Drain-Source Voltage		V_{DS}	600		V
Gate-Source Voltage		V_{GS}	±30		V
Drain Current	T_C=25°C	I_D	11		A
	T_C=100°C		7		
Drain Current Pulsed		I_{DM}	44		A
Power Dissipation (T_C=25°C)		P_D	22	89	W
- Derate above 25°C			0.18	0.71	W/°C
Single Pulsed Avalanche Energy (Note1)		E_{AS}	310		mJ
Reverse diode dv/dt (Note 2)		dv/dt	15		V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	50		V/ns
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value		Unit
		SVSP11N60FJD2	SVSP11N60DD2	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	5.68	1.40	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.50	62.0	°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_C=25°C)

Characteristics	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA		600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V		--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V		--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA		2.0	--	4.0	V
Static Drain- Source on State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=5.5A	Tj=25°C	--	0.30	0.36	Ω
			Tj=125°C		0.62		
Gate resistance	R_g	f=1MHz			5.2		Ω
Input Capacitance	C_{iss}	f=1MHz,V_{GS}=0V, V_{DS}=100V		--	634	--	pF
Output Capacitance	C_{oss}			--	38	--	
Reverse Transfer Capacitance	C_{rss}			--	2.6	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V, V_{GS}=10V, R_G=10Ω, I_D=11A (Note 2,3)		--	10	--	ns
Turn-on Rise Time	t_r			--	29	--	
Turn-off Delay Time	$t_{d(off)}$			--	37	--	
Turn-off Fall Time	t_f			--	23	--	
Total Gate Charge	Q_g	V_{DD}=480V, V_{GS}=10V, I_D=11A (Note 2,3)		--	22	--	nC
Gate-Source Charge	Q_{gs}			--	5.0	--	
Gate-Drain Charge	Q_{gd}			--	11	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	11	A
Pulsed Source Current	I_{SM}		--	--	44	
Diode Forward Voltage	V_{SD}	I_S=11A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	V_{DD}=50V, I_F=11A , dI_F/dt=100A/μs (注 2)	--	371	--	ns
Reverse Recovery Charge	Q_{rr}		--	3.8	--	μC

Notes:

1. L=79mH,I_{AS}=2.6A,V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V,I_{SD}<=11A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

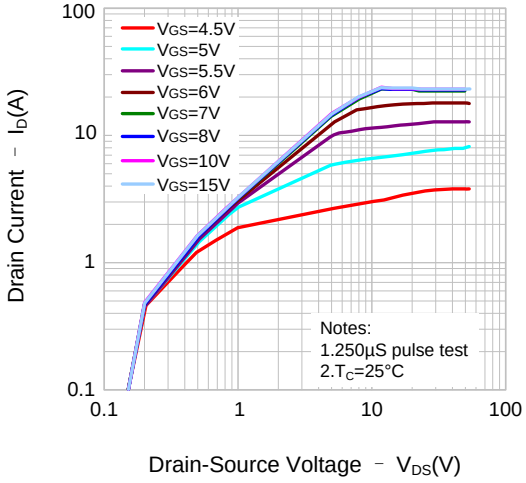


Figure 2. Transfer Characteristics

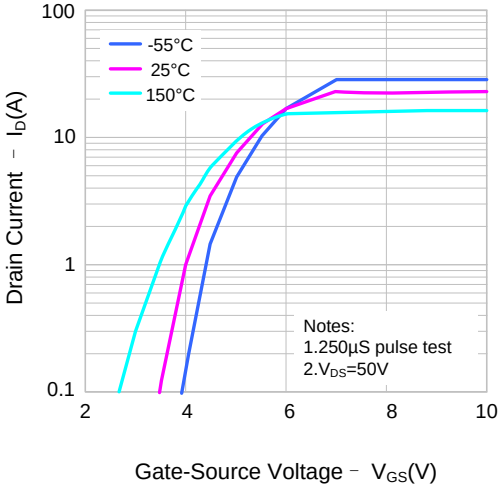


Figure 3. On-Resistance Variation vs. Drain Current

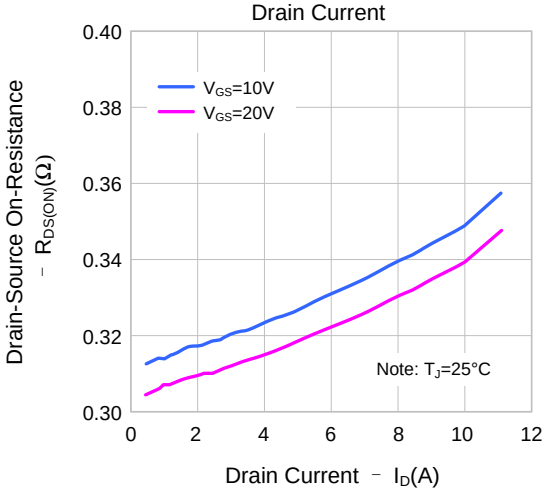


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

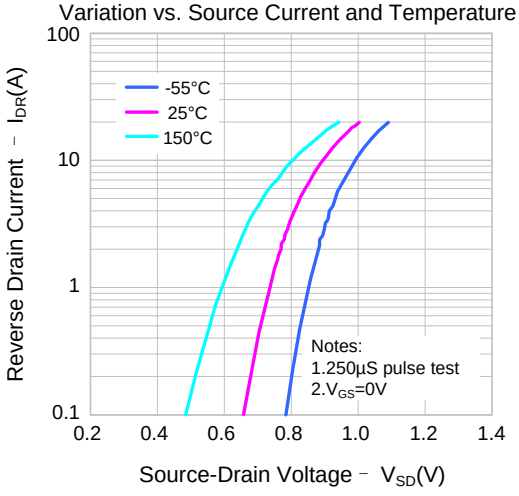


Figure 5. Capacitance Characteristics

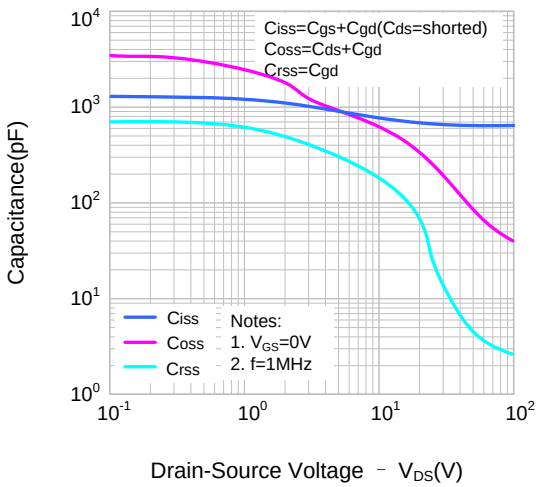
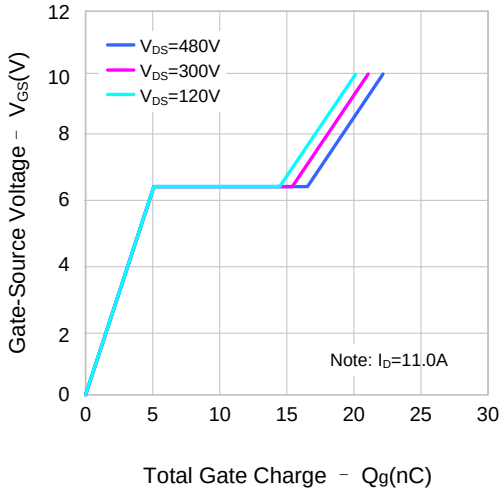


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

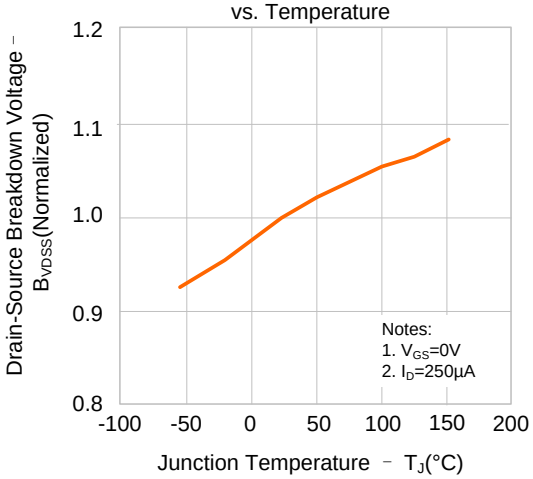


Figure 8. On-resistance Variation vs. Temperature

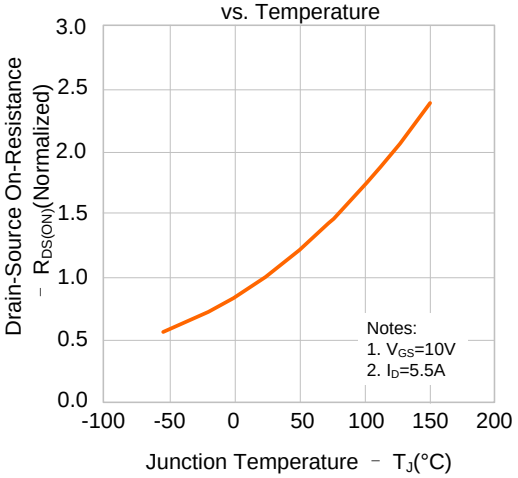


Figure 9-1. Max. Safe Operating Area (SVSP11N60FJD2)

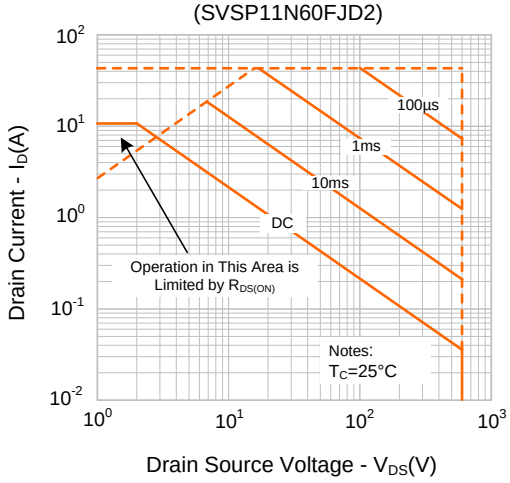
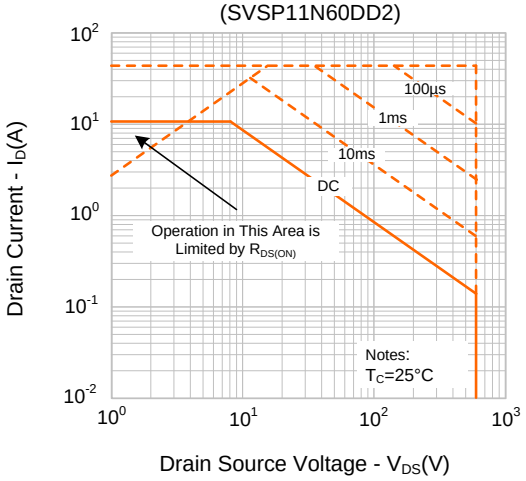
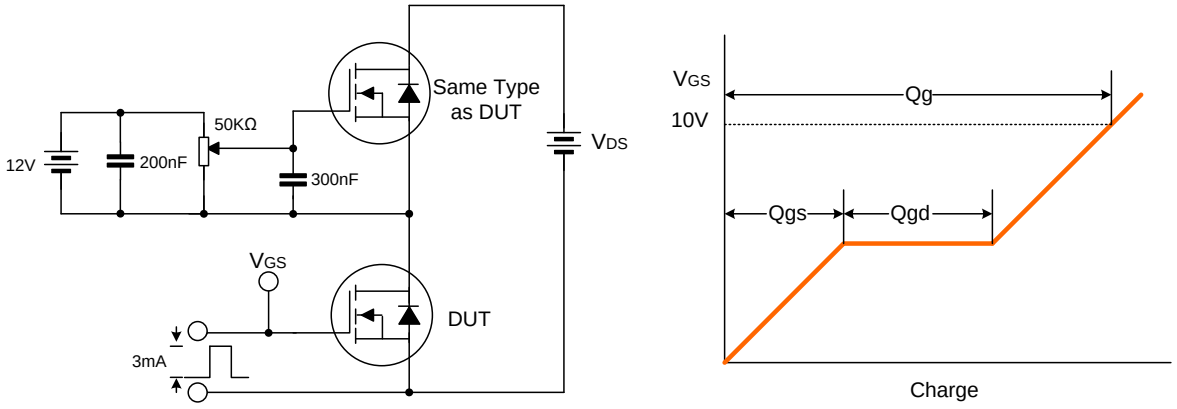


Figure 9-2 Max. Safe Operating Area (SVSP11N60DD2)

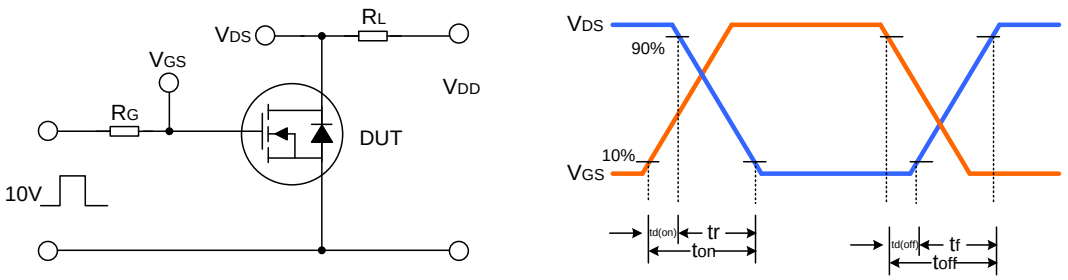


TYPICAL TEST CIRCUIT

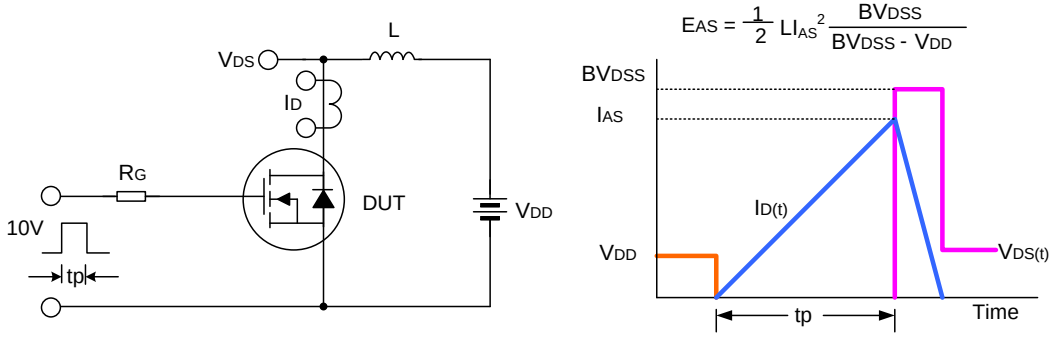
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



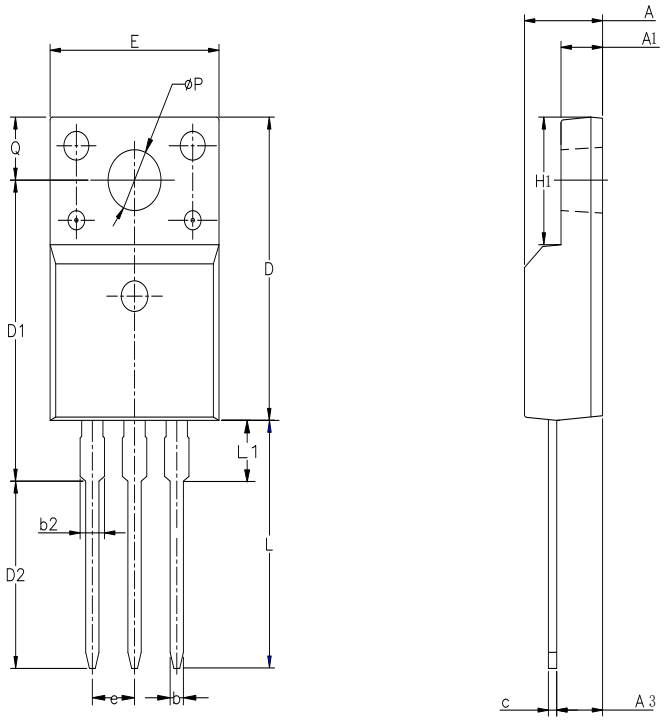
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220FJ-3L

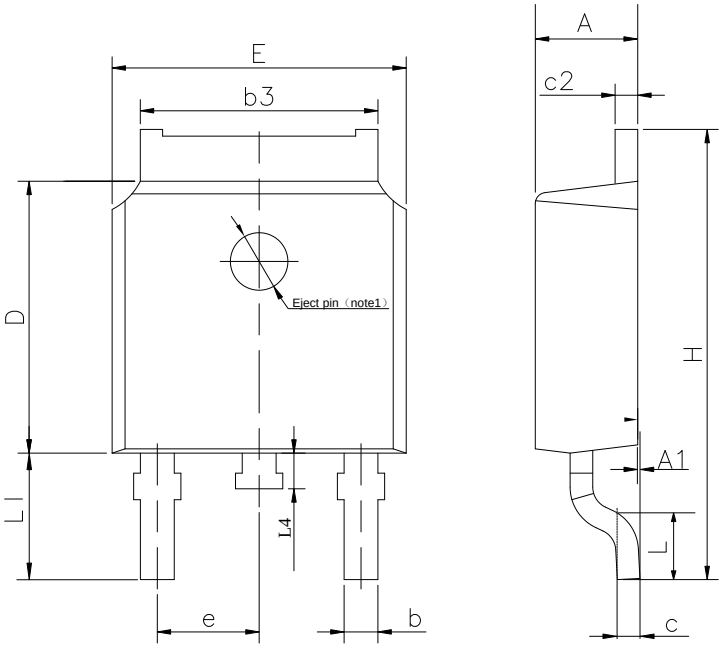
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
øP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-252-2L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

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Part No.:	SVSP11N60FJ(D)D2	Document Type:	Datasheet
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Rev.: 1.3

Revision History:

1. Modify Electrical characteristics and Fig 5,6

Rev.: 1.2

Revision History:

1. Modify the value of Rg

Rev.: 1.1

Revision History:

1. Add the package outline of TO-252-2L

Rev.: 1.0

Revision History:

1. First release