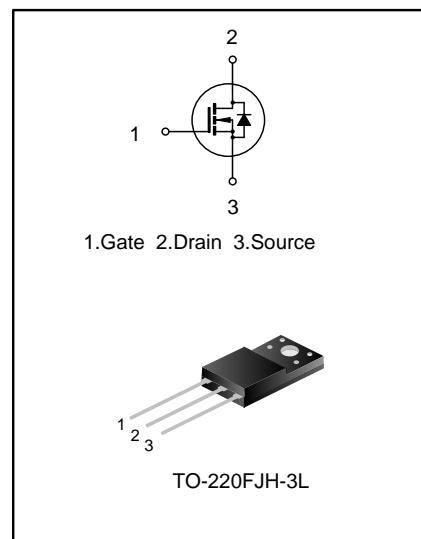


14A, 650V SUPER JUNCTION MOS POWER TRANSISTOR

DESCRIPTION

SVSP14N65FJHE2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's super junction MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.



FEATURES

- ◆ 14A, 650V, $R_{DS(on)(typ.)}=0.26\Omega @ V_{GS}=10V$
- ◆ New revolutionary high voltage technology
- ◆ Ultra low gate charge
- ◆ Periodic avalanche rated
- ◆ Extreme dv/dt rated
- ◆ High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVSP14N65FJHE2	TO-220FJH-3L	P14N65FJHE	Halogen free	Tube



ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_c=25^\circ\text{C}$)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 30	V
Drain Current	$T_c=25^\circ\text{C}$	I_D	14	A
	$T_c=100^\circ\text{C}$		8.8	
Drain Current Pulsed		I_{DM}	56	A
Power Dissipation ($T_c=25^\circ\text{C}$) - Derate above 25°C		P_D	39	W
			0.3	$\text{W}/^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	593	mJ
Reverse diode dv/dt (Note 2)		dv/dt	15	V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	50	V/ns
Operation Junction Temperature Range		T_J	-55~+150	$^\circ\text{C}$
Storage Temperature Range		T_{stg}	-55~+150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.2	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$



ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_c=25^\circ\text{C}$)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{\text{DS}}=650\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 30\text{V}, V_{\text{DS}}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}, I_{\text{D}}=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source on State Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=7.0\text{A}$	--	0.26	0.31	Ω
Gate resistance	R_g	$f=1\text{MHz}$	--	7.1	--	Ω
Input Capacitance	C_{iss}	$f=1\text{MHz}, V_{\text{GS}}=0\text{V}, V_{\text{DS}}=100\text{V}$	--	768	--	pF
Output Capacitance	C_{oss}		--	46	--	
Reverse Transfer Capacitance	C_{rss}		--	1.6	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=325\text{V}, V_{\text{GS}}=10\text{V}, R_g=24\Omega, I_{\text{D}}=14\text{A}$	--	14	--	ns
Turn-on Rise Time	t_r		--	37	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	47	--	
Turn-off Fall Time	t_f		--	34	--	
Total Gate Charge	Q_g	$V_{\text{DD}}=520\text{V}, V_{\text{GS}}=10\text{V}, I_{\text{D}}=14\text{A}$	--	19	--	nC
Gate-Source Charge	Q_{gs}		--	5.9	--	
Gate-Drain Charge	Q_{gd}		--	7.7	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_s	Integral Reverse P-N Junction Diode in the MOSFET	--	--	14	A
Pulsed Source Current	I_{SM}		--	--	56	
Diode Forward Voltage	V_{SD}	$I_s=14\text{A}, V_{\text{GS}}=0\text{V}$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_s=14\text{A}, V_{\text{GS}}=0\text{V}, dI_F/dt=100\text{A}/\mu\text{s}$	--	365	--	ns
Reverse Recovery Charge	Q_{rr}		--	4.4	--	

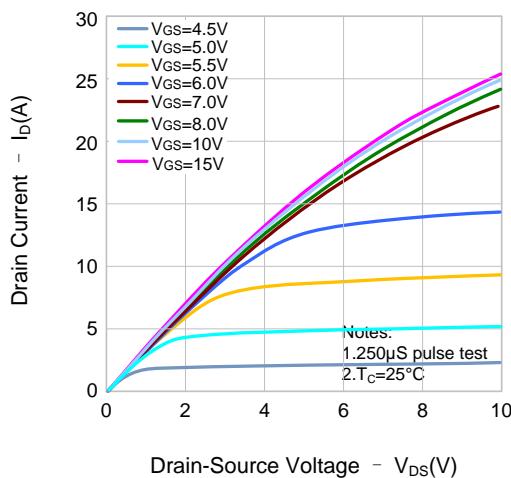
Notes:

1. $L=79\text{mH}, I_{\text{AS}}=3.6\text{A}, V_{\text{DD}}=100\text{V}, R_g=25\Omega$, starting temperature $T_j=25^\circ\text{C}$;
2. $V_{\text{DS}}=0\sim 400\text{V}, I_{\text{SD}} \leq 14\text{A}, T_j=25^\circ\text{C}$;
3. $V_{\text{DS}}=0\sim 480\text{V}$;
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$;
5. Essentially independent of operating temperature.



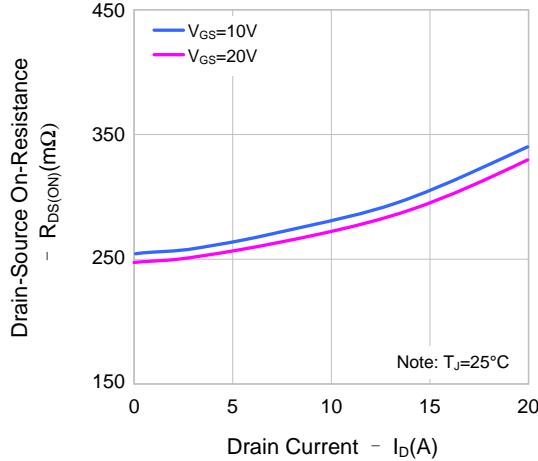
TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics



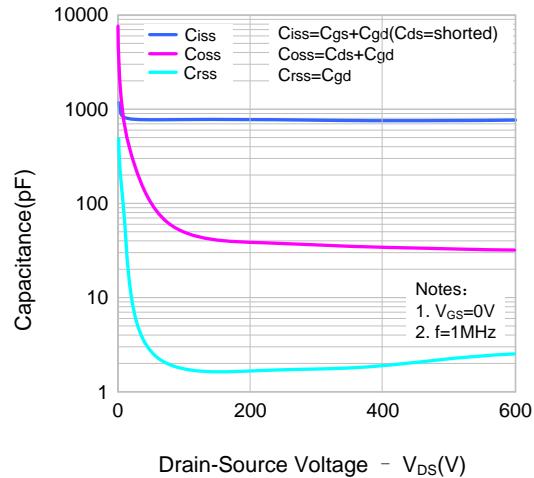
Drain-Source Voltage - V_{DS} (V)

Figure 3. On-Resistance Variation vs.
Drain Current



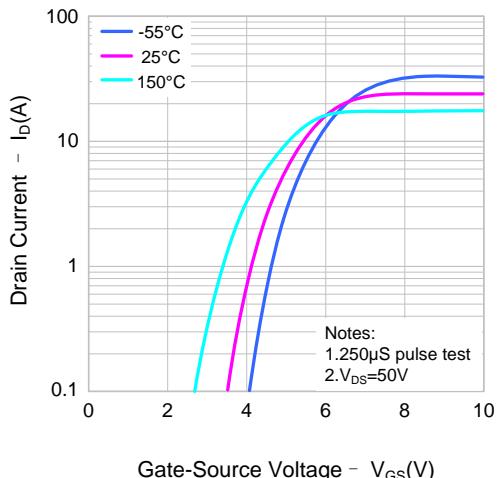
Drain Current - I_D (A)

Figure 5. Capacitance Characteristics



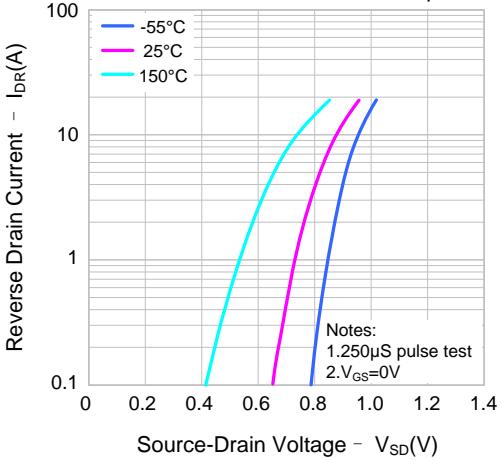
Drain-Source Voltage - V_{DS} (V)

Figure 2. Transfer Characteristics



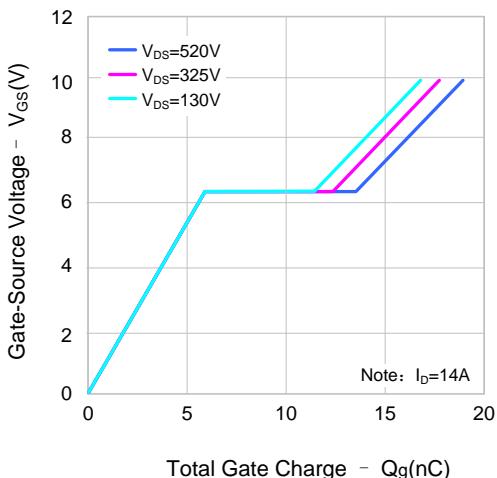
Gate-Source Voltage - V_{GS} (V)

Figure 4. Body Diode Forward Voltage
Variation vs. Source Current and Temperature



Source-Drain Voltage - V_{SD} (V)

Figure 6. Gate Charge Characteristics



Total Gate Charge - Q_g (nC)



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

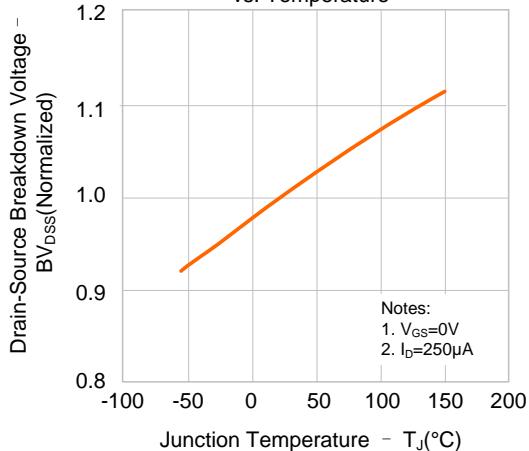


Figure 8. On-resistance Variation vs. Temperature

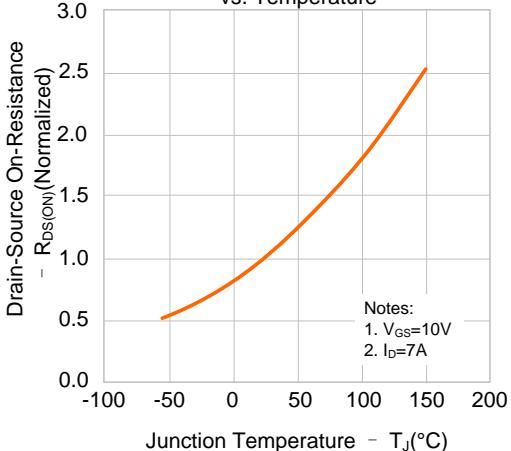
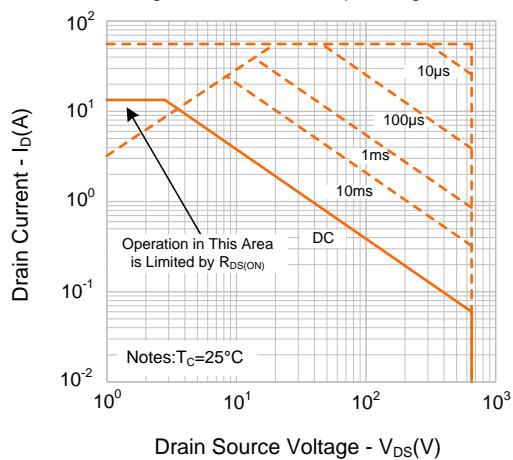
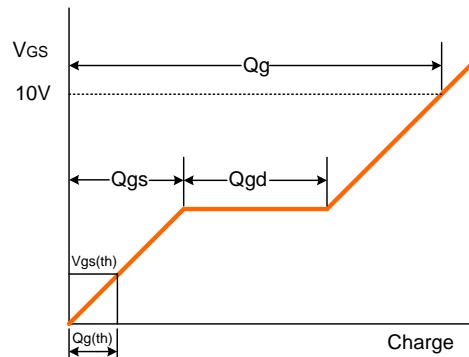
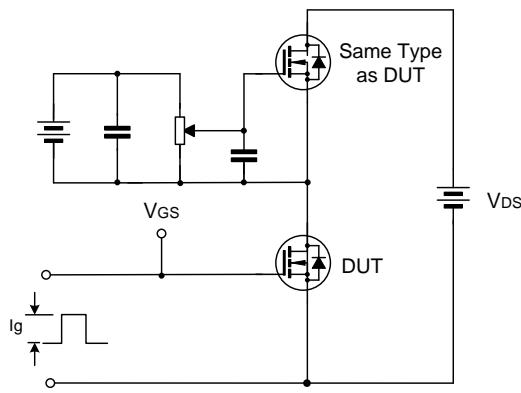


Figure 9. Max. Safe Operating Area

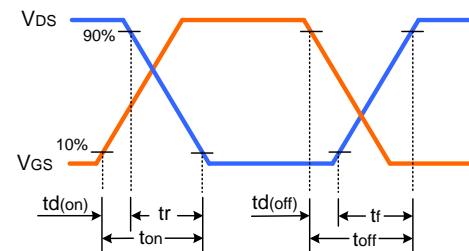
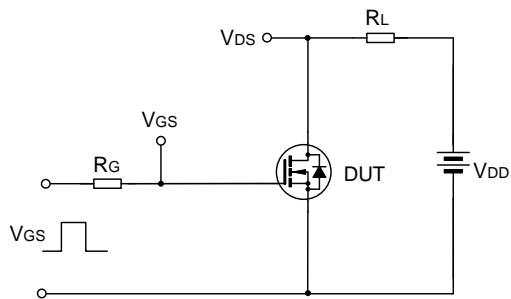




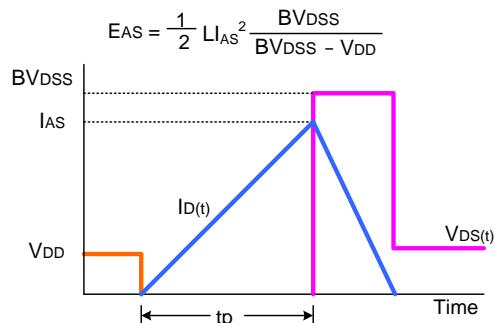
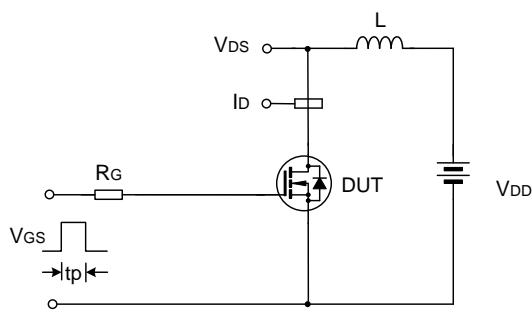
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



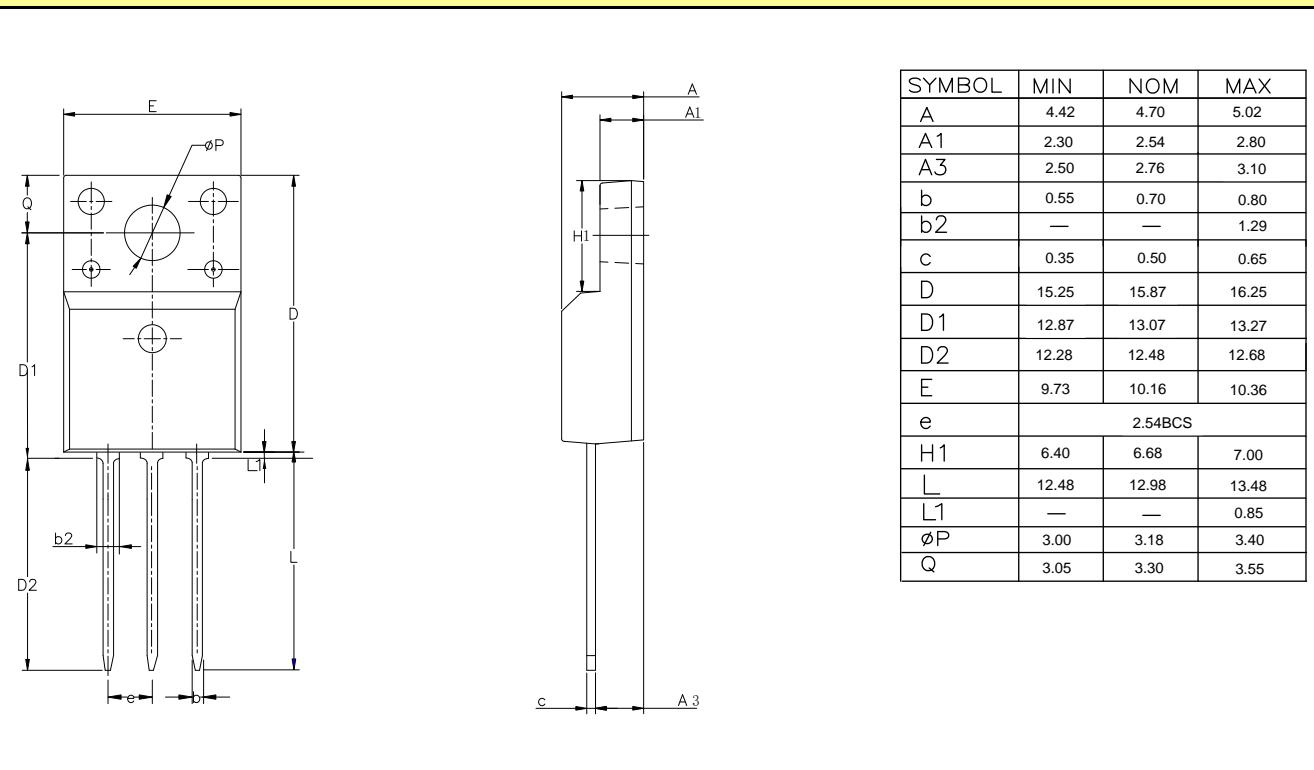
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220FJH-3L

UNIT: mm



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SVSP14N65FJHE2_Datasheet

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Rev.: 1.1

Revision History:

1. Update Electrical schematic and typical test circuit
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Rev.: 1.0

Revision History:

1. First release
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