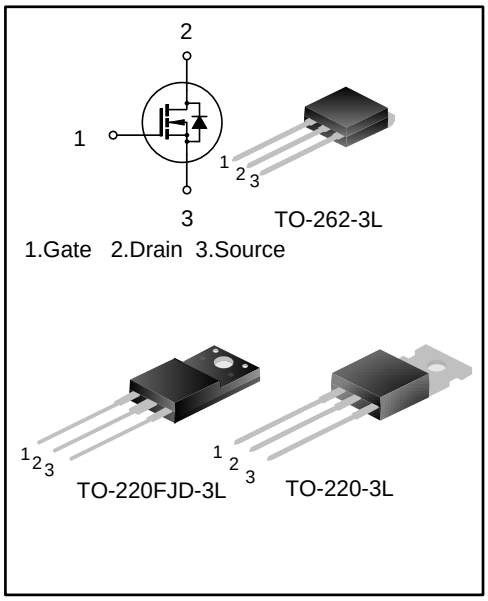
14A, 650V SUPER JUNCTION MOS POWER TRANSISTOR

DESCRIPTION

SVSP14N65FJD/T/KD2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's DPMOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.



FEATURES

- 14A,650V, $R_{DS(on)(typ.)}$=0.26Ω@V_{GS}=10V
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVSP14N65FJDD2	TO-220FJD-3L	P14N65FJD	Halogen free	Tube
SVSP14N65TD2	TO-220-3L	P14N65TD2	Halogen free	Tube
SVSP14N65KD2	TO-262-3L	P14N65KD2	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_A=25°C)

Characteristics		Symbol	Ratings		Unit
			SVSP14N65FJDD2	SVSP14N65TD2/KD2	
Drain-Source Voltage		V_{DS}	650		V
Gate-Source Voltage		V_{GS}	±30		V
Drain Current	T_C=25°C	I_D	14		A
	T_C=100°C		8.8		
Drain Current Pulsed		I_{DM}	56		A
Power Dissipation (T_C=25°C)		P_D	35.7	139	W
- Derate above 25°C			0.29	1.1	W/°C
Single Pulsed Avalanche Energy (Note1)		E_{AS}	593		mJ
Reverse diode dv/dt (Note 2)		dv/dt	15		V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	50		V/ns
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value		Unit
		SVSP14N65FJDD2	SVSP14N65TD2/KD2	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.50	0.9	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_j=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source on State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=7.0A	--	0.26	0.31	Ω
Gate resistance	R_g	f=1MHz	--	2.7	--	Ω
Input Capacitance	C_{iss}	f=1MHz,V_{GS}=0V, V_{DS}=100V	--	802	--	pF
Output Capacitance	C_{oss}		--	45	--	
Reverse Transfer Capacitance	C_{rss}		--	2.5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V, V_{GS}=10V, R_G=24Ω, I_D=14A (Note 4,5)	--	13	--	ns
Turn-on Rise Time	t_r		--	37	--	
Turn-off Delay Time	$t_{d(off)}$		--	59	--	
Turn-off Fall Time	t_f		--	32	--	
Total Gate Charge	Q_g	V_{DD}=520V, V_{GS}=10V, I_D=14A (Note 4,5)	--	24	--	nC
Gate-Source Charge	Q_{gs}		--	6.5	--	
Gate-Drain Charge	Q_{gd}		--	11	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	14	A
Pulsed Source Current	I_{SM}		--	--	56	
Diode Forward Voltage	V_{SD}	I_S=14A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	V_{DD}=50V, I_F=14A , dI_F/dt=100A/μs (Note 4)	--	367	--	ns
Reverse Recovery Charge	Q_{rr}		--	4.7	--	μC

Notes:

1. L=79mH,I_{AS}=3.6A,V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V,I_{SD}<=14A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

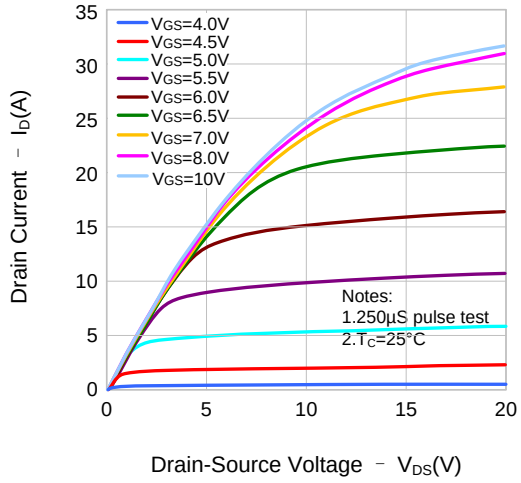


Figure 2. Transfer Characteristics

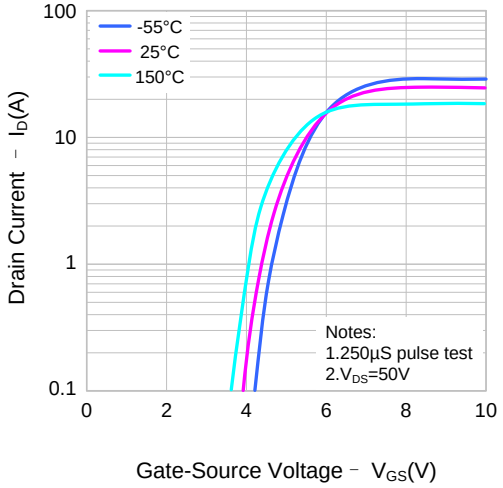


Figure 3. On-Resistance Variation vs. Drain Current

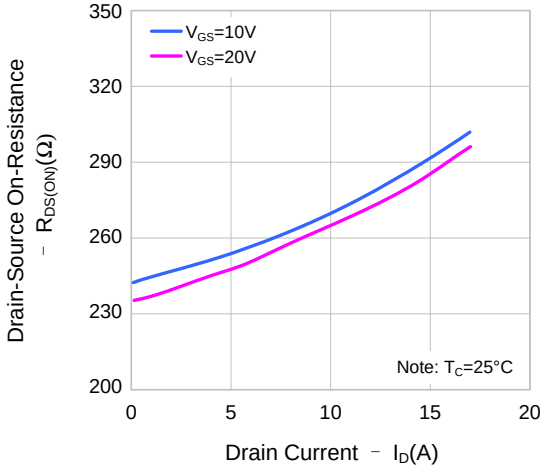


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

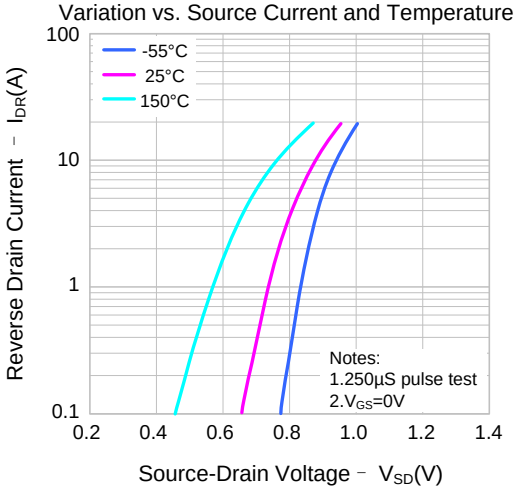


Figure 5. Capacitance Characteristics

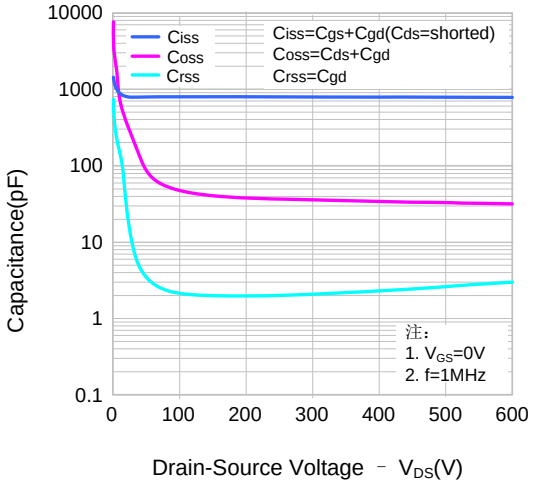
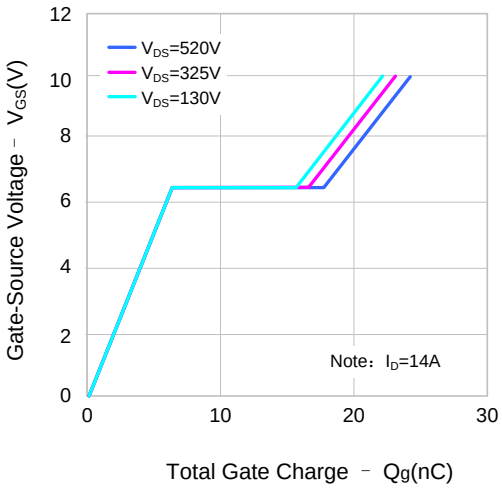


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

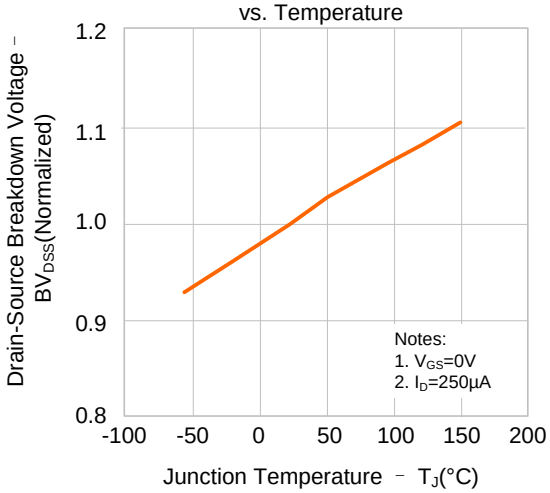


Figure 8. On-resistance Variation vs. Temperature

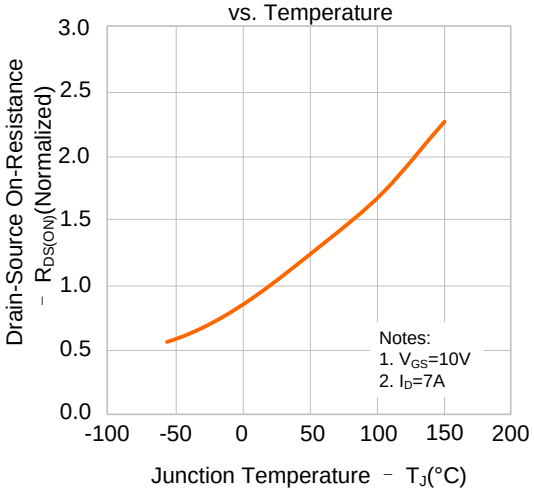


Figure 9-1. Max. Safe Operating Area (SVSP14N65FJDD2)

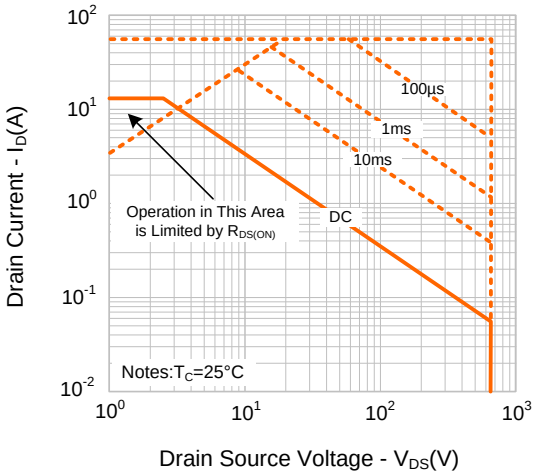
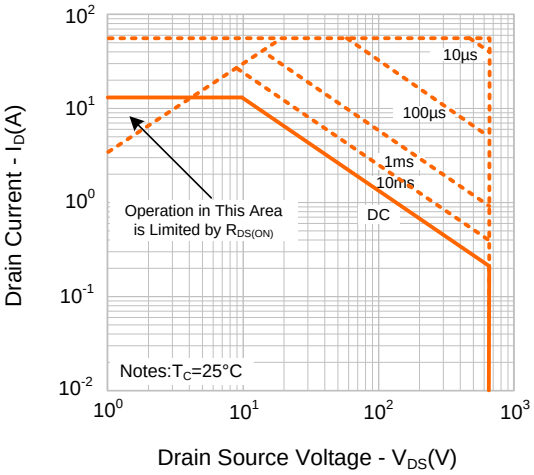
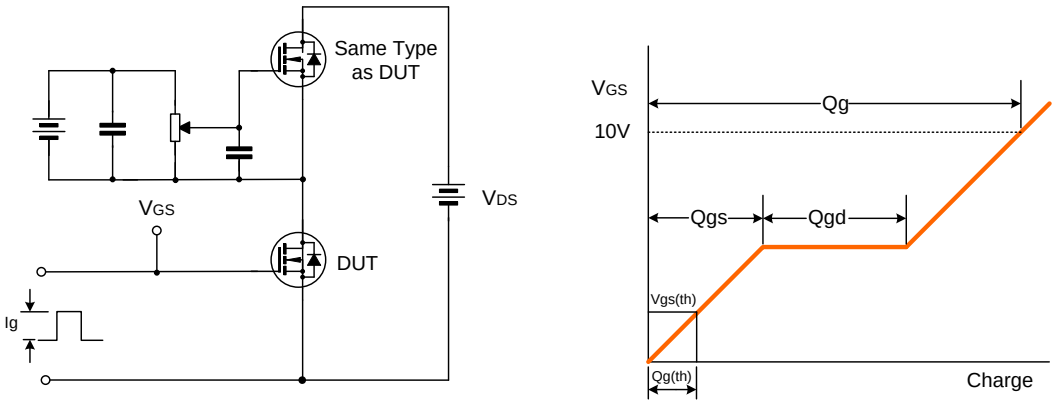


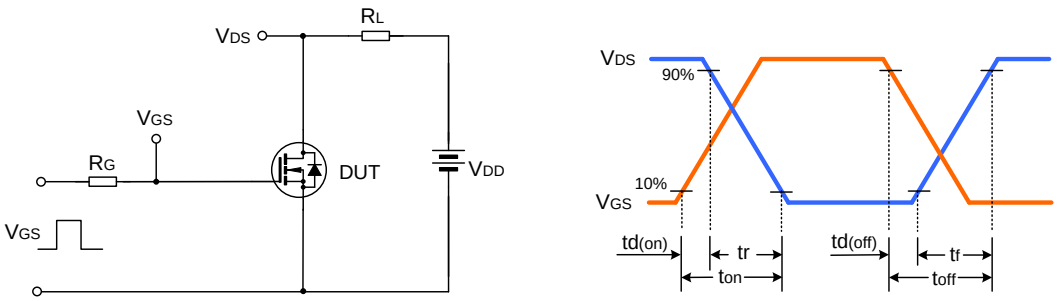
Figure 9-2. Max. Safe Operating Area (SVSP14N65T/KD2)



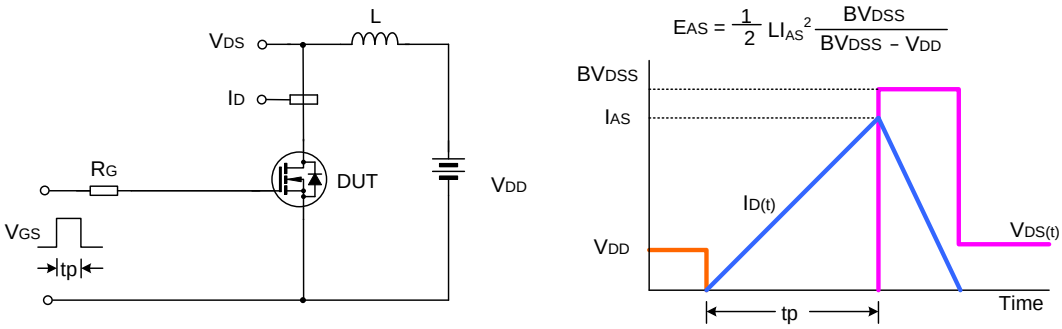
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



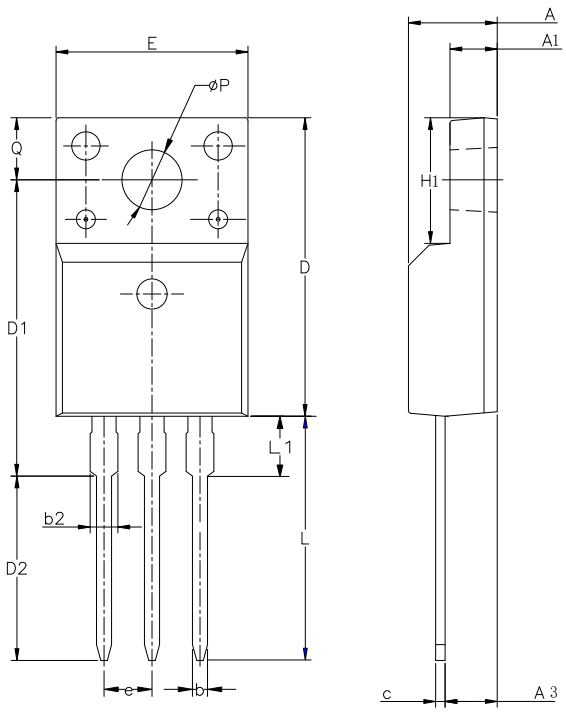
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform

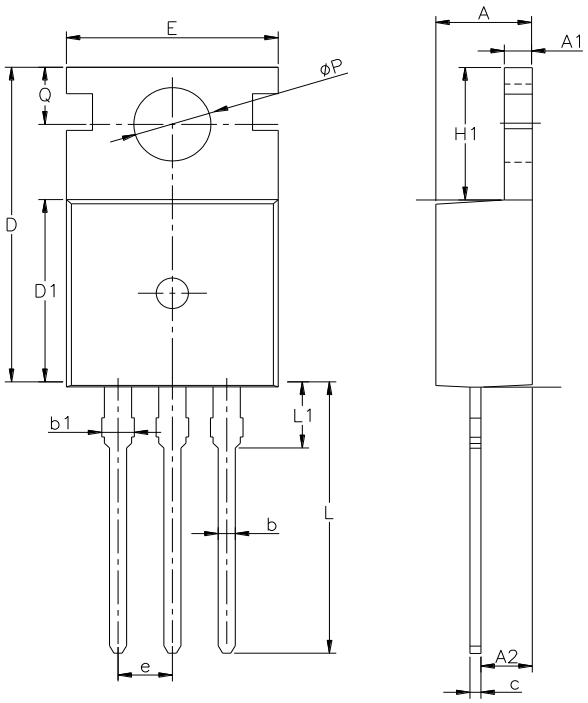
PACKAGE OUTLINE

TO-220FJD-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e		2.54BCS	
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

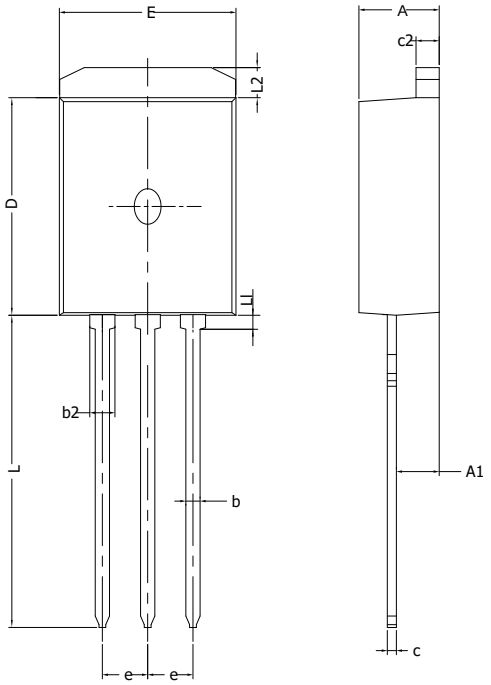
TO-220-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e		2.54BSC	
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ØP	3.40	3.70	3.90
Q	2.60	—	3.20

PACKAGE OUTLINE(CONTINUED)

TO-262-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	---	2.92
b	0.71	0.80	0.90
b2	1.20	---	1.50
c	0.34	---	0.65
c2	1.22	1.30	1.35
D	8.38	---	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	---	14.10
L1	---	---	0.75
L2	1.12	---	1.42

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Rev.: 1.3

Revision History:

1. Modify Electrical schematic and TYPICAL TEST CIRCUIT
2. Update Fig 5

Rev.: 1.2

Revision History:

1. Modify Test conditions of I_{GSS}

Rev.: 1.1

Revision History:

1. Add SVSP14N65TD2、SVSP14N65KD2

Rev.: 1.0

Revision History:

1. First release