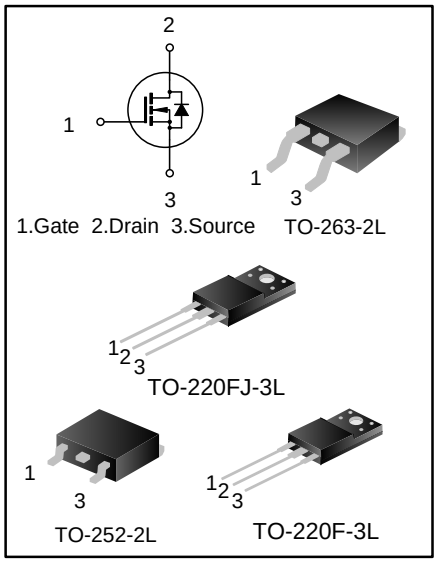
11A, 650V SUPER JUNCTION MOS POWER TRANSISTOR

DESCRIPTION

SVS11N65D/F/S/FJD2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's super junction MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior.
Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.



FEATURES

- 11A,650V, $R_{DS(on)(typ.)}$=0.33Ω@V_{GS}=10V
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVS11N65DD2TR	TO-252-2L	11N65DD2	Halogen free	Tape & Reel
SVS11N65FD2	TO-220F-3L	11N65FD2	Halogen free	Tube
SVS11N65SD2	TO-263-2L	11N65SD2	Halogen free	Tube
SVS11N65SD2TR	TO-263-2L	11N65SD2	Halogen free	Tape & Reel
SVS11N65FJD2	TO-220FJ-3L	11N65FJD2	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics		Symbol	Ratings			Unit
			SVS11N65 DD2	SVS11N65 F/FJD2	SVS11N65 SD2	
Drain-Source Voltage		V_{DS}	650			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	11			A
	T_C=100°C		7			
Drain Current Pulsed		I_{DM}	44			A
Power Dissipation (T_C=25°C)		P_D	87	35	92	W
- Derate above 25°C			0.70	0.28	0.74	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	250			mJ
Reverse Diode dv/dt	(Note 2)	dv/dt	15			V/ns
MOSFET dv/dt Ruggedness	(Note 3)	dv/dt	50			V/ns
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVS11N65 DD2	SVS11N65 F/FJD2	SVS11N65 SD2	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.44	3.57	1.36	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.0	62.5	62.50	°C/W

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source on State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=5.5A	--	0.33	0.4	Ω
Gate Resistance	R_g	f=1MHz	--	5.2	--	Ω
Input Capacitance	C_{iss}	f=1MHz, V_{GS}=0V, V_{DS}=100V	--	632	--	pF
Output Capacitance	C_{oss}		--	37	--	
Reverse Transfer Capacitance	C_{rss}		--	2.3	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V, V_{GS}=10V, R_G=24Ω, I_D=11A (Note 4,5)	--	12	--	ns
Turn-on Rise Time	t_r		--	35	--	
Turn-off Delay Time	$t_{d(off)}$		--	64	--	
Turn-off Fall Time	t_f		--	31	--	
Total Gate Charge	Q_g	V_{DD}=520V, V_{GS}=10V, I_D=11A (Note 4,5)	--	23	--	nC
Gate-Source Charge	Q_{gs}		--	5.3	--	
Gate-Drain Charge	Q_{gd}		--	11	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	11	A
Pulsed Source Current	I_{SM}		--	--	44	
Diode Forward Voltage	V_{SD}	I_S=11A, V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=11A, V_{GS}=0V, dI_F/dt=100A/μs (Note 4)	--	361	--	ns
Reverse Recovery Charge	Q_{rr}		--	3.9	--	μC

Notes:

1. L=79mH, I_{AS}=2.4A, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V, I_{SD}<=11A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

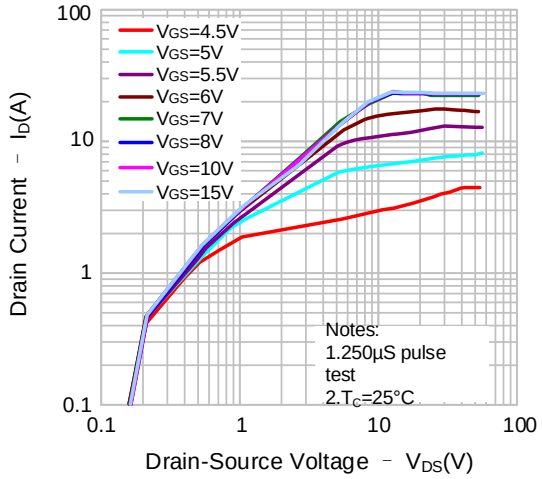


Figure 2. Transfer Characteristics

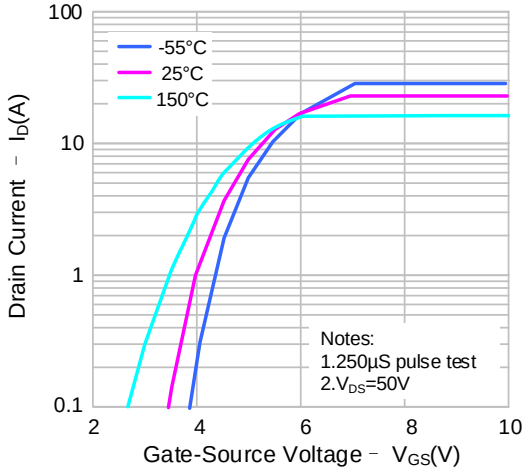


Figure 3. On-Resistance Variation vs. Drain Current

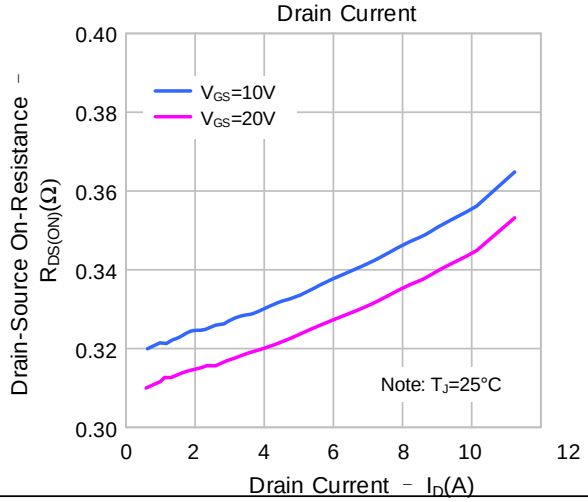


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

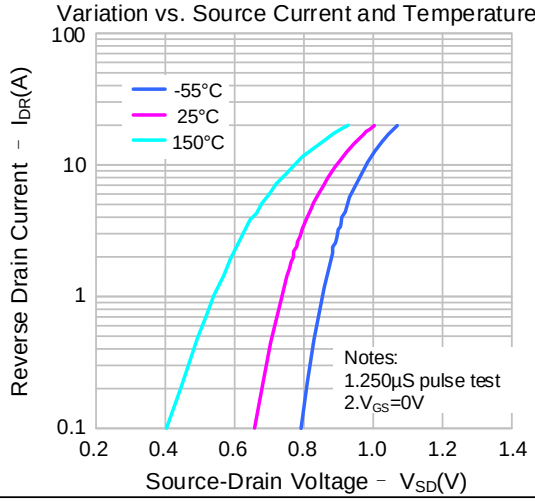


Figure 5. Capacitance Characteristics

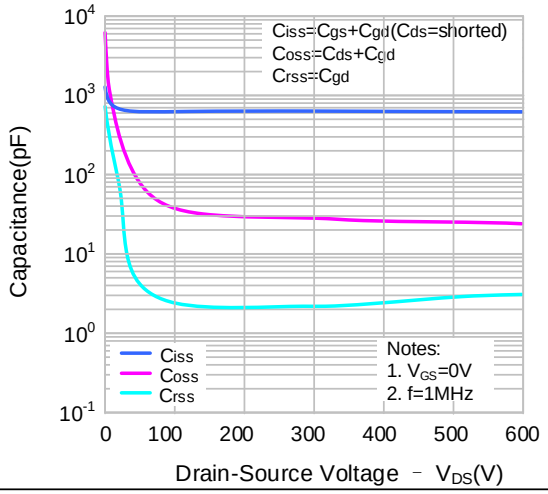
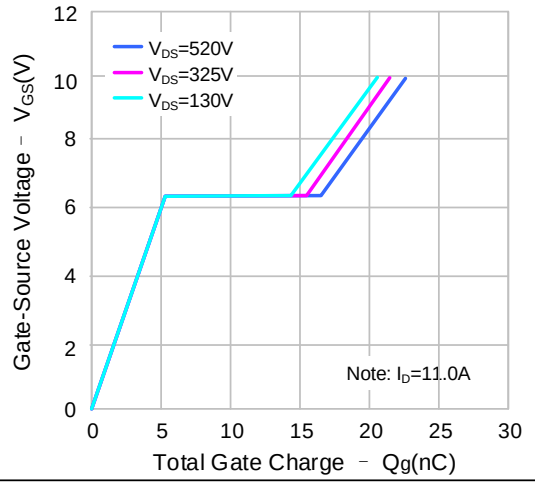


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

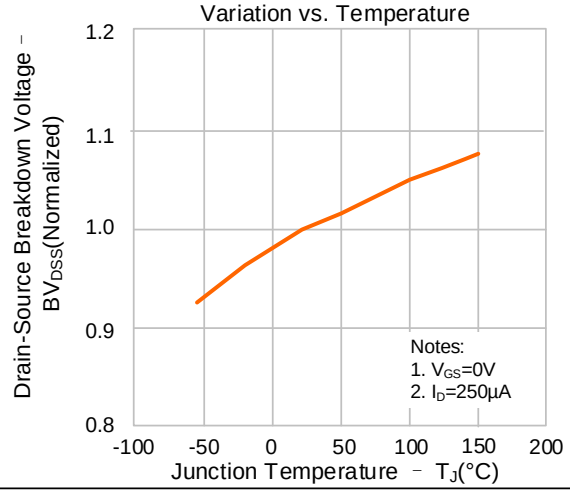


Figure 8. On-resistance Variation vs. Temperature

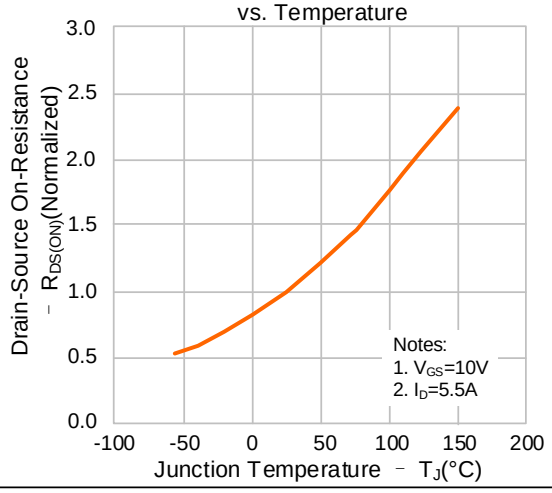


Figure 9.1. Max. Safe Operating Area(SVS11N65DD2)

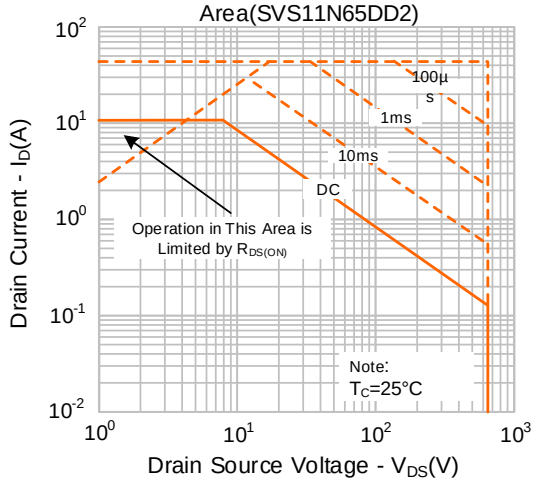


Figure 9.2. Max. Safe Operating Area(SVS11N65F/FJD2)

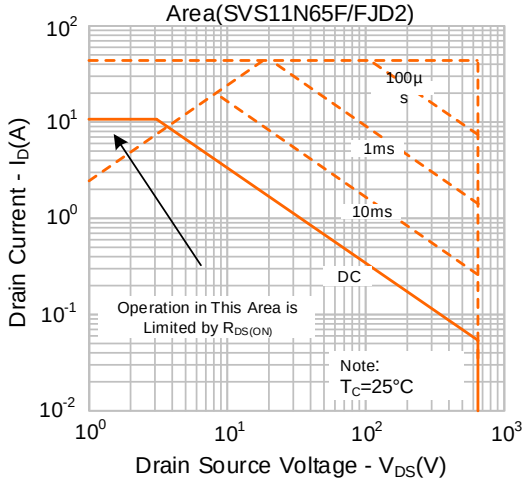
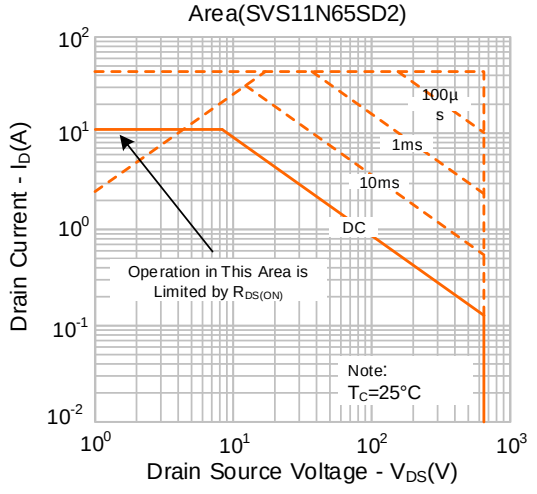
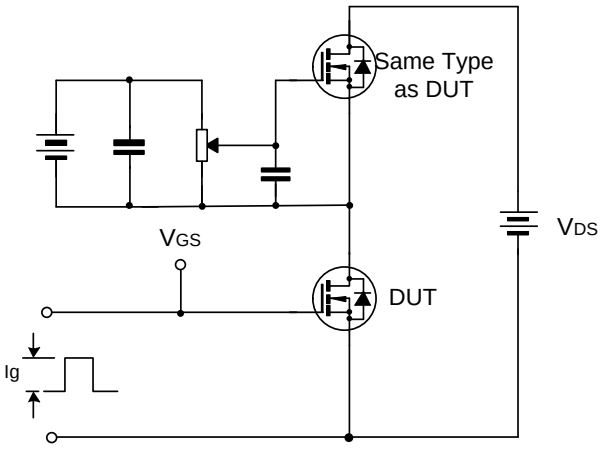


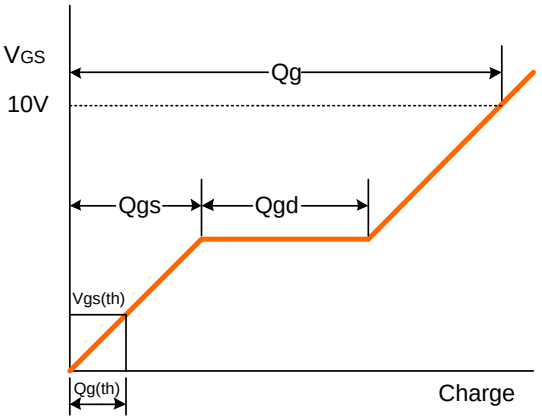
Figure 9.3. Max. Safe Operating Area(SVS11N65SD2)



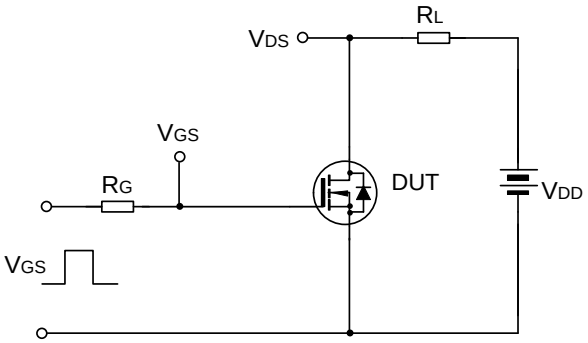
TYPICAL TEST CIRCUIT

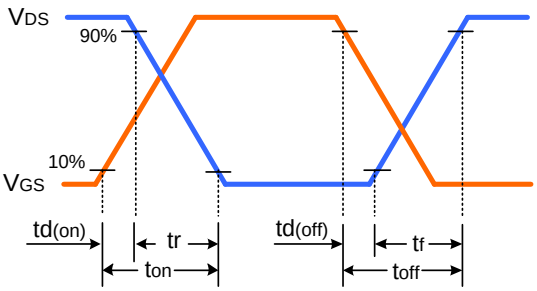
Gate Charge Test Circuit & Waveform



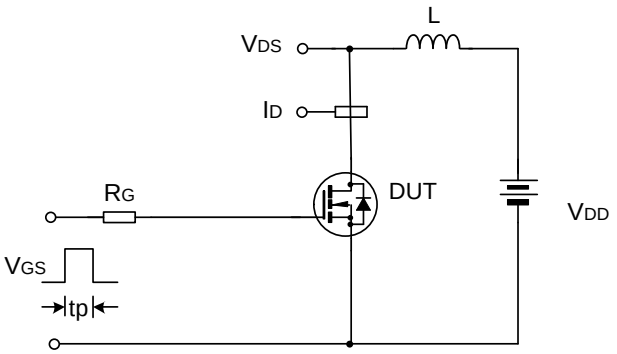


Resistive Switching Test Circuit & Waveform

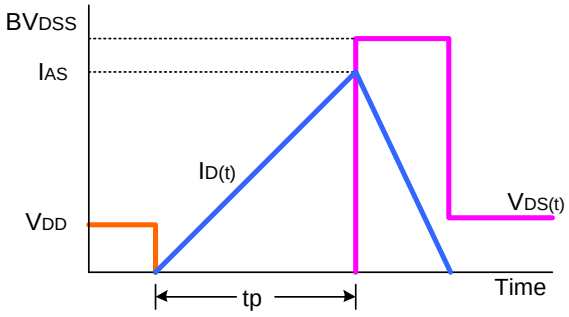




Unclamped Inductive Switching Test Circuit & Waveform



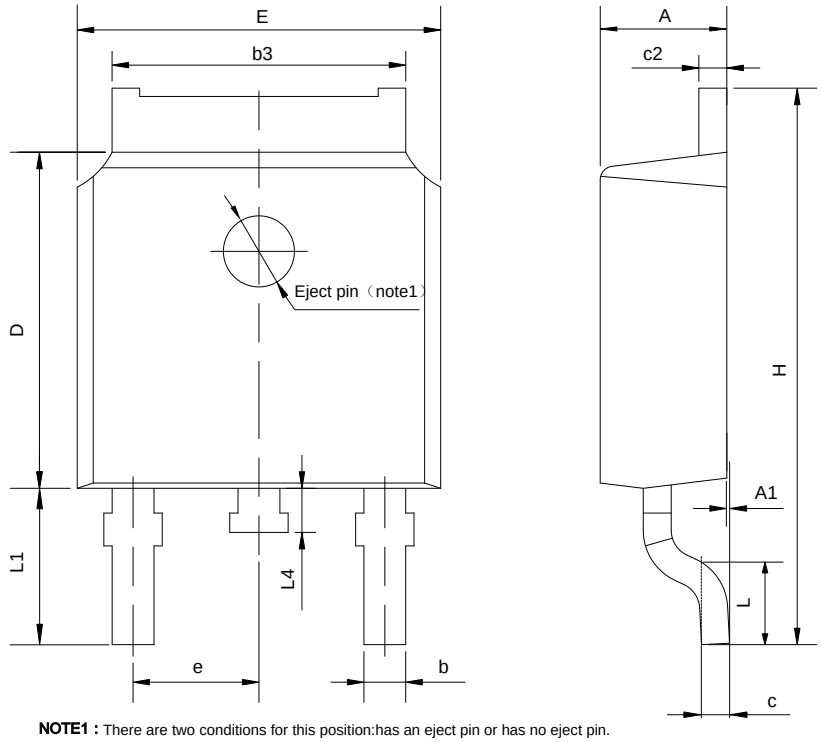
$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



PACKAGE OUTLINE

TO-252-2L

UNIT: mm

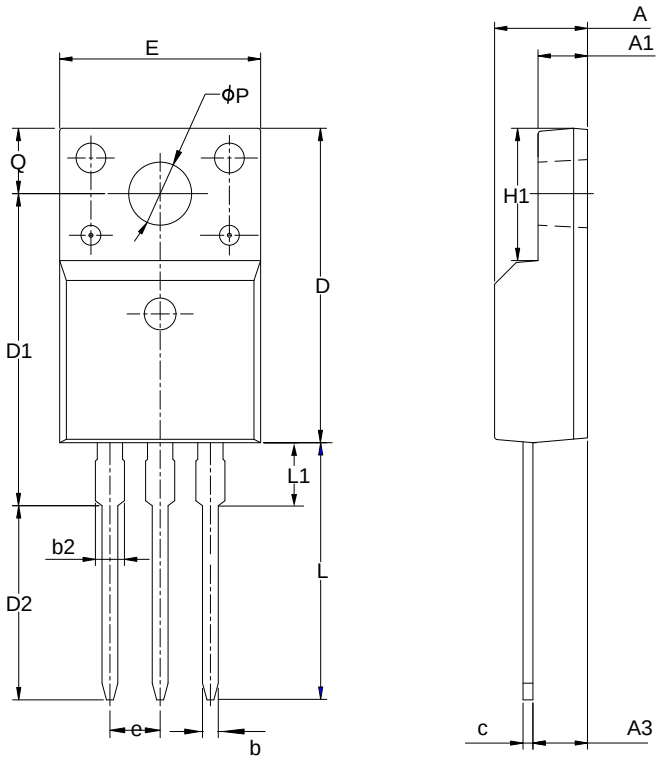


NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

TO-220F-3L

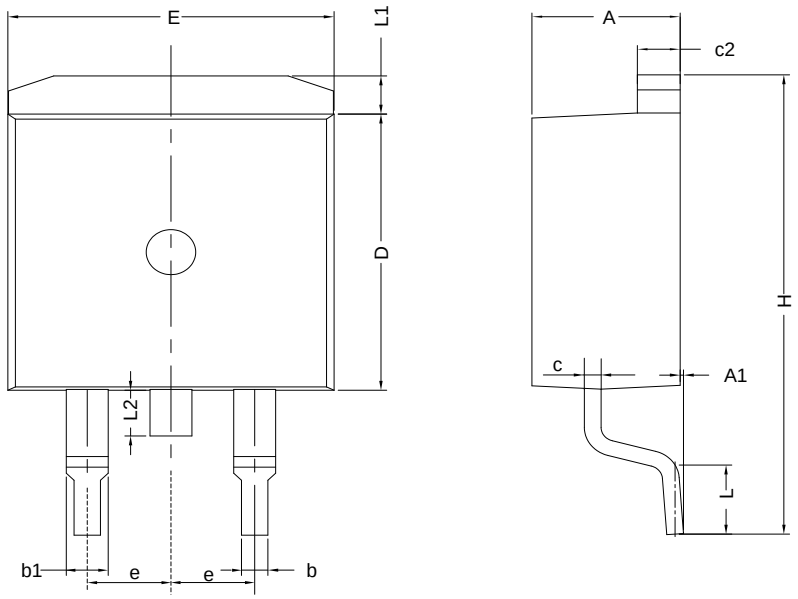
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	–	–	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	–	–	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

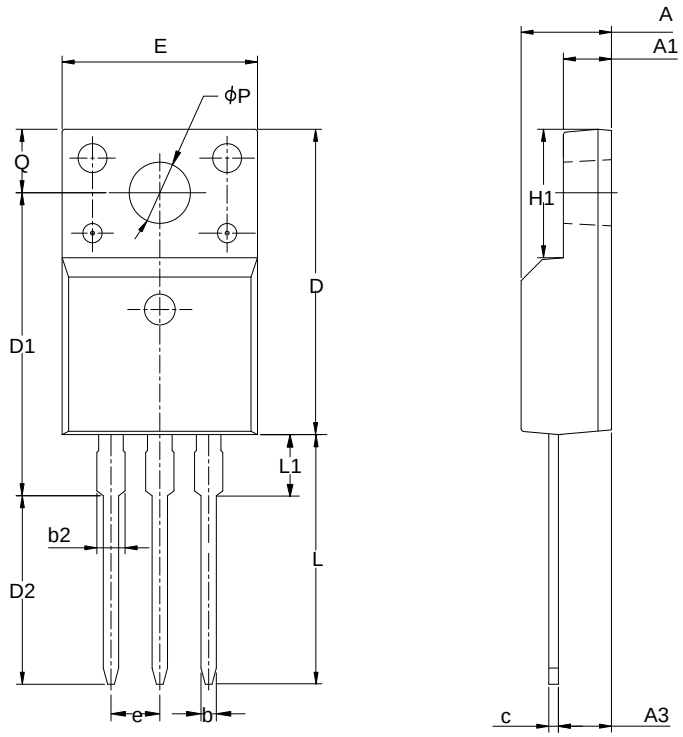
PACKAGE OUTLINE(continued)

TO-263-2L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
b1	1.17	—	1.50
c	0.30	—	0.60
c2	1.17	1.27	1.37
D	8.50	—	9.35
E	9.80	—	10.45
e	2.54BSC		
H	14.70	—	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	—	—	1.75

TO-220FJ-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

Important notice :

1. Silan reserves the right to make changes of this instruction without notice.
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Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http: //www.silan.com.cn

Rev.: 1.7

Revision History:

1. Update curve template
2. Update typical test circuit
3. Update package outline
4. Update important notice

Rev.: 1.6

Revision History:

1. Update Electrical schematic and TYPICAL TEST CIRCUIT
2. Update Fig 5

Rev.: 1.5

Revision History:

1. Add dv/dt
2. Update Fig 5 and 6
3. Add TO-220FJ-3L

Rev.: 1.4

Revision History:

1. Modify the figure 3

Rev.: 1.3

Revision History:

1. Modify the absolute maximum ratings
2. Modify the thermal characteristics

Rev.: 1.2

Revision History:

1. Add the package information of TO-263-2L

Rev.: 1.1

Revision History:

1. Add the package information of TO-220F-3L

Rev.: 1.0

Revision History:

1. First release