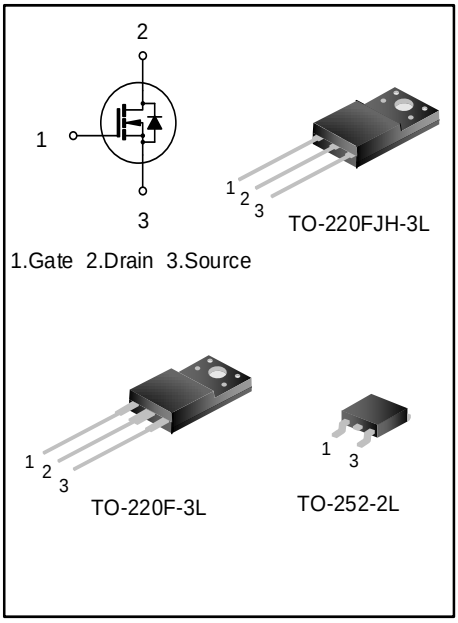
5A, 650V SUPER JUNCTION MOS POWER TRANSISTOR

GENERAL DESCRIPTION

SVS5N65F(D)(FJH)D2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's super junction MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior. Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.



FEATURES

- 5A, 650V, $R_{DS(on)(typ.)}$=0.78Ω@V_{GS}=10V
- New revolutionary high voltage technology
- Ultra low gate charge
- Enhanced avalanche capability
- Extreme dv/dt rated
- High peak current capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVS5N65FD2	TO-220F-3L	SVS5N65FD2	Halogen free	Tube
SVS5N65DD2TR	TO-252-2L	SVS5N65DD2	Halogen free	Tape&Reel
SVS5N65FJHD2	TO-220FJH-3L	5N65FJHD2	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_J=25°C unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SVS5N65FD2/FJHD2	SVS5N65DD2	
Drain-Source Voltage		V_{DS}	650		V
Gate-Source Voltage		V_{GS}	±30		V
Drain Current	T_C=25°C	I_D	5.0		A
	T_C=100°C		3.2		
Drain Current Pulsed		I_{DM}	20		A
Power Dissipation(T_C=25°C)		P_D	27	42	W
-Derate above 25°C			0.22	0.28	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	214		mJ
Reverse diode dv/dt (Note 2)		dv/dt	15		V/ns
MOSFET dv/dt ruggedness (Note 3)		dv/dt	50		V/ns
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVS5N65FD2/FJHD2	SVS5N65DD2	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4.6	3.57	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.50	62.0	°C/W

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain-Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2.5A	--	0.78	0.96	Ω
Gate resistance	R_g	f=1.0MHz	--	7.2	--	Ω
Input Capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V, f=1.0MHz	--	301	--	pF
Output Capacitance	C_{oss}		--	19	--	
Reverse Transfer Capacitance	C_{rss}		--	2.3	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V, I_D=5.0A, V_{GS}=10V, R_G=24Ω (Note 4,5)	--	8.6	--	ns
Turn-on Rise Time	t_r		--	26	--	
Turn-off Delay Time	$t_{d(off)}$		--	31	--	
Turn-off Fall Time	t_f		--	24	--	
Total Gate Charge	Q_g	V_{DS}=520V, I_D=5.0A, V_{GS}=10V (Note 4,5)	--	12	--	nC
Gate-Source Charge	Q_{gs}		--	2.9	--	
Gate-Drain Charge	Q_{gd}		--	6.7	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	5.0	A
Pulsed Source Current	I_{SM}		--	--	20.0	
Diode Forward Voltage	V_{SD}	I_S=5.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=5.0A,V_{GS}=0V, dI_F/dt=100A/μs (Note 4)	--	336	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.0	--	μC

Notes:

1. L=79mH,I_{AS}=2.2A,V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. V_{DS}=0~400V,I_{SD}<=5.0A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

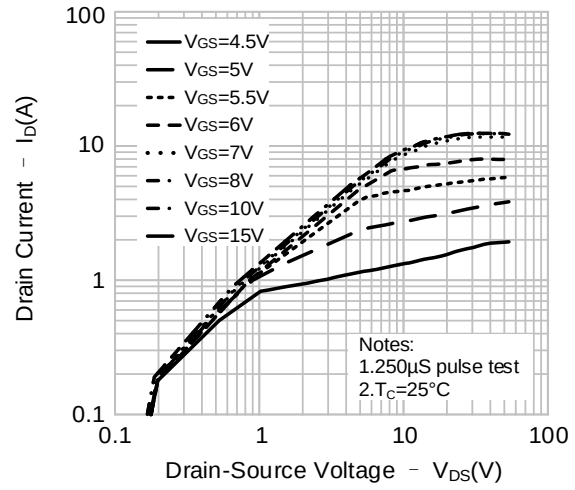


Figure 2. Transfer Characteristics

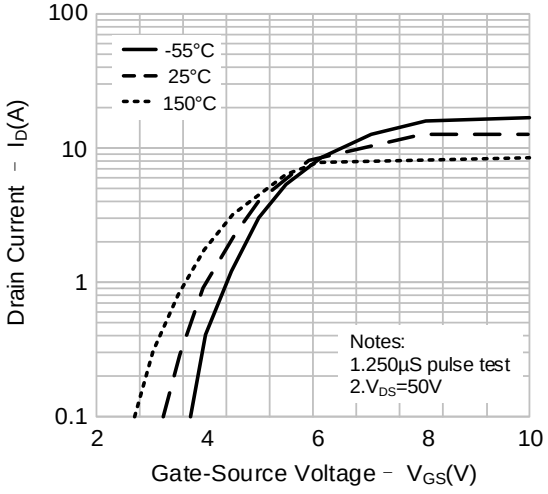


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

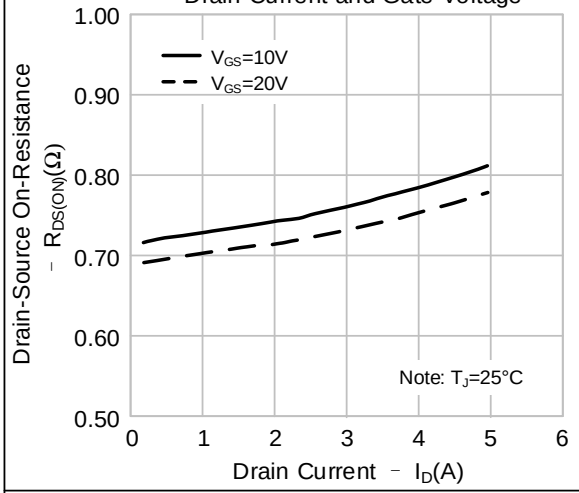


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

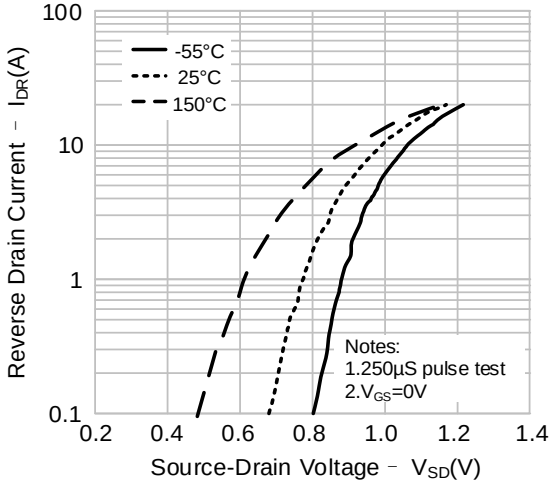


Figure 5. Capacitance Characteristics

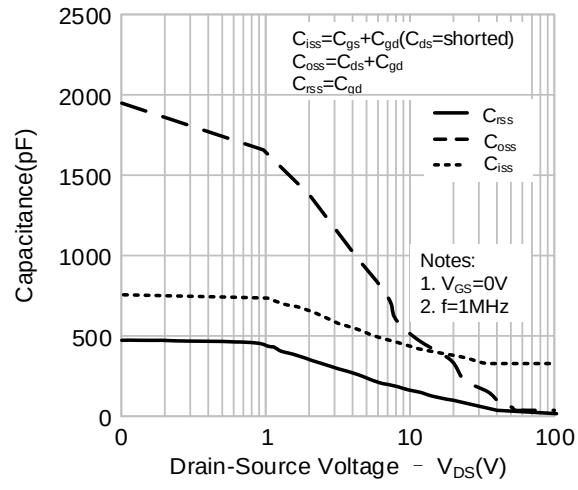
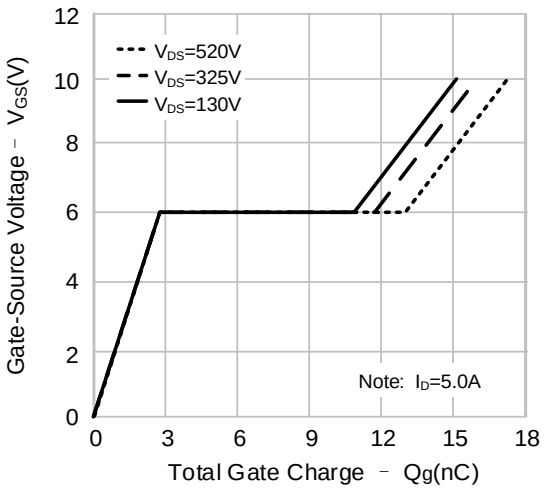


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

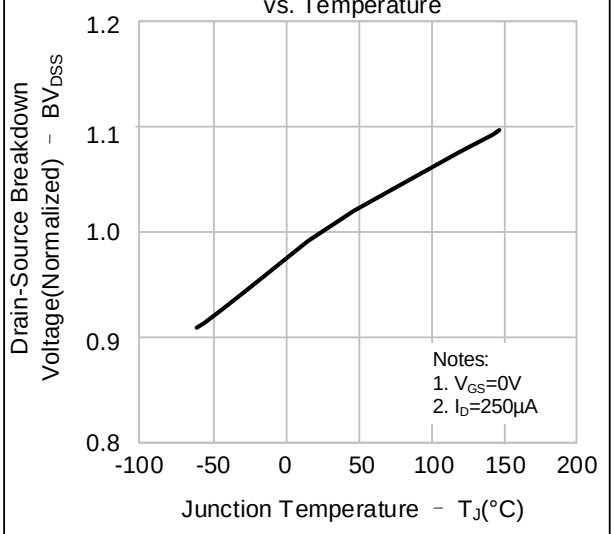


Figure 8. On-resistance Variation vs. Temperature

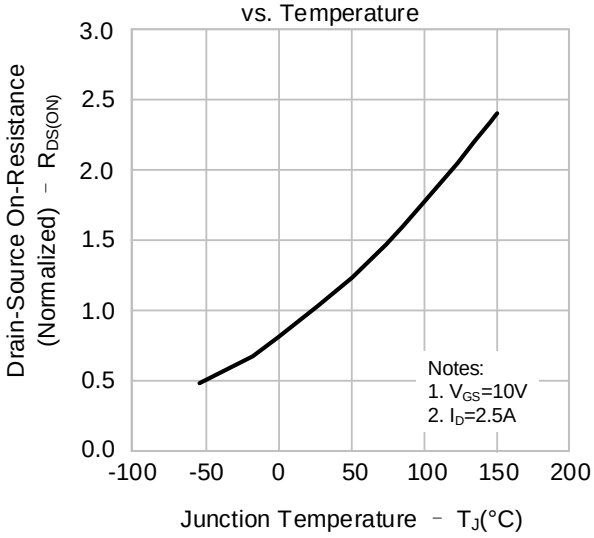


Figure 9-1. Max. Safe Operating Area(SVS5N65F/FJHD2)

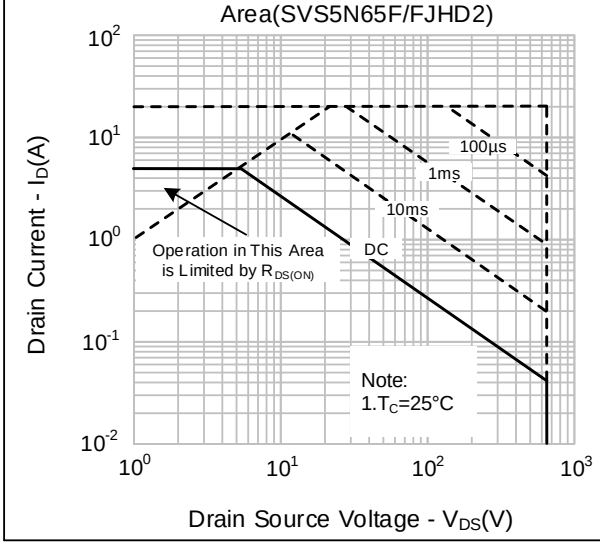
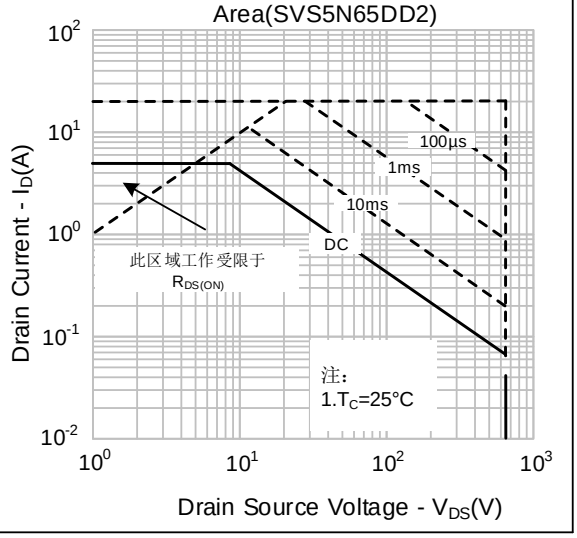
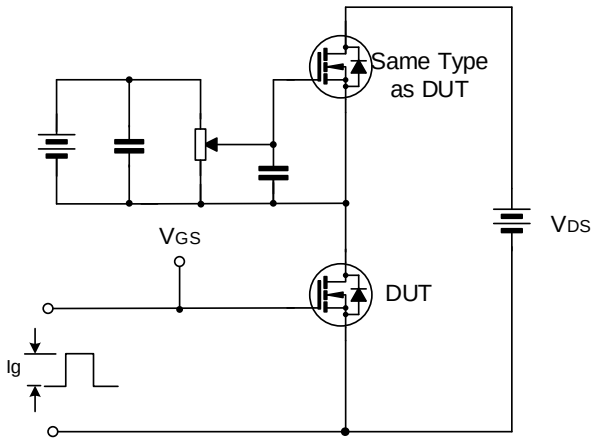


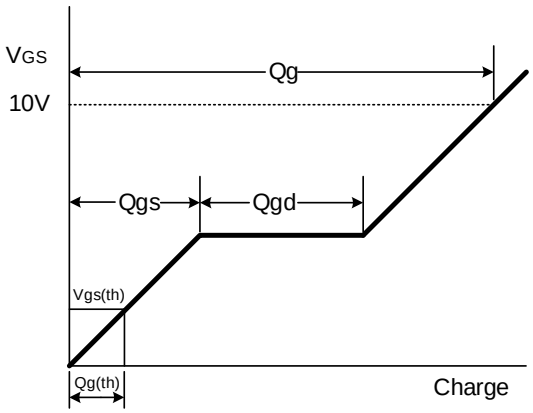
Figure 9-2. Max. Safe Operating Area(SVS5N65DD2)



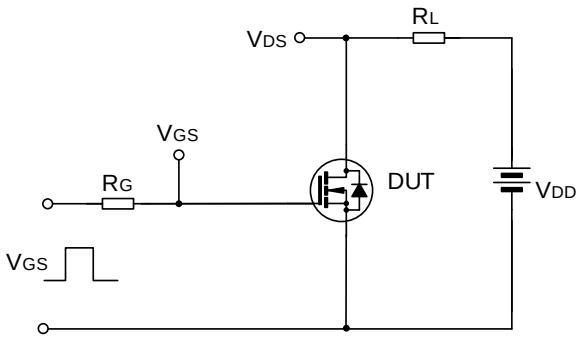
TYPICAL TEST CIRCUIT

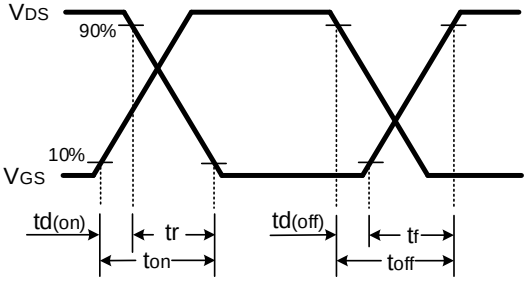
Gate Charge Test Circuit & Waveform



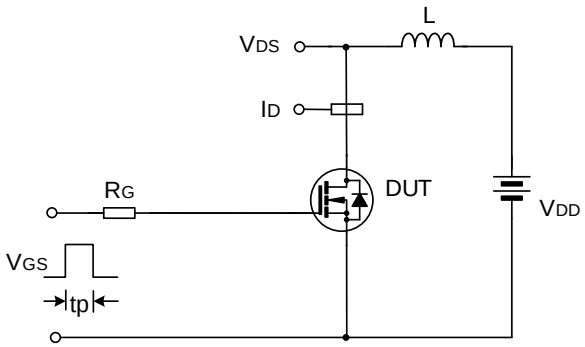


Resistive Switching Test Circuit & Waveform

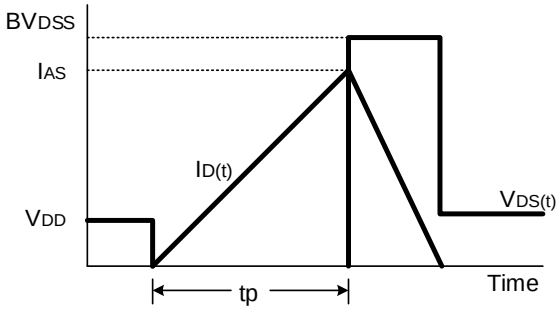




Unclamped Inductive Switching Test Circuit & Waveform



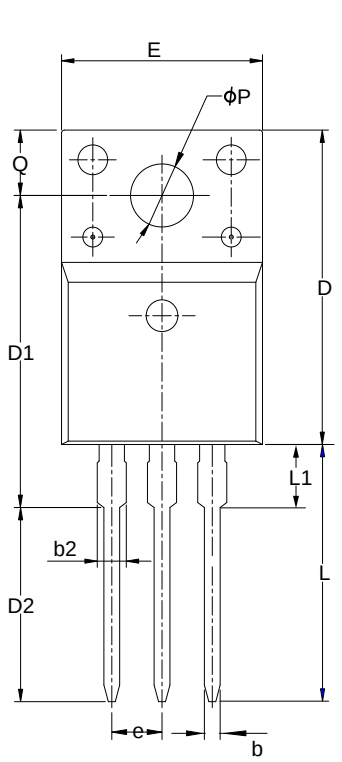
$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

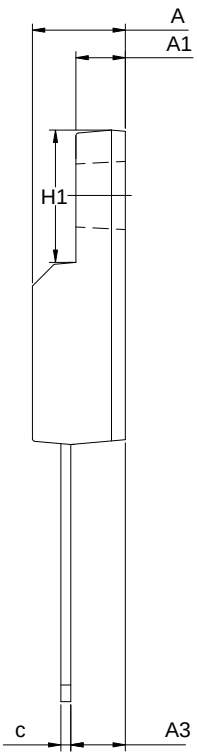


PACKAGE OUTLINE

TO-220F-3L

UNIT: mm

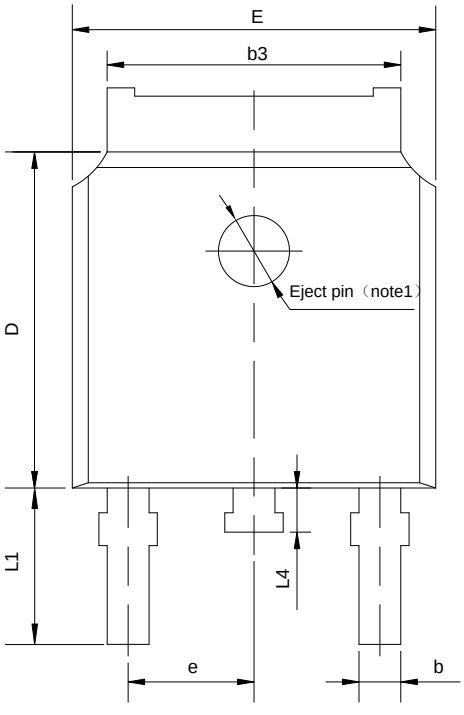


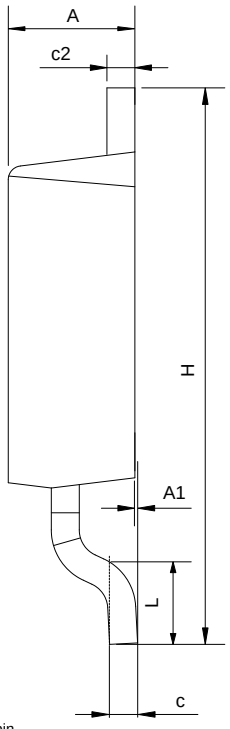


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	–	–	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	–	–	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-252-2L

UNIT: mm



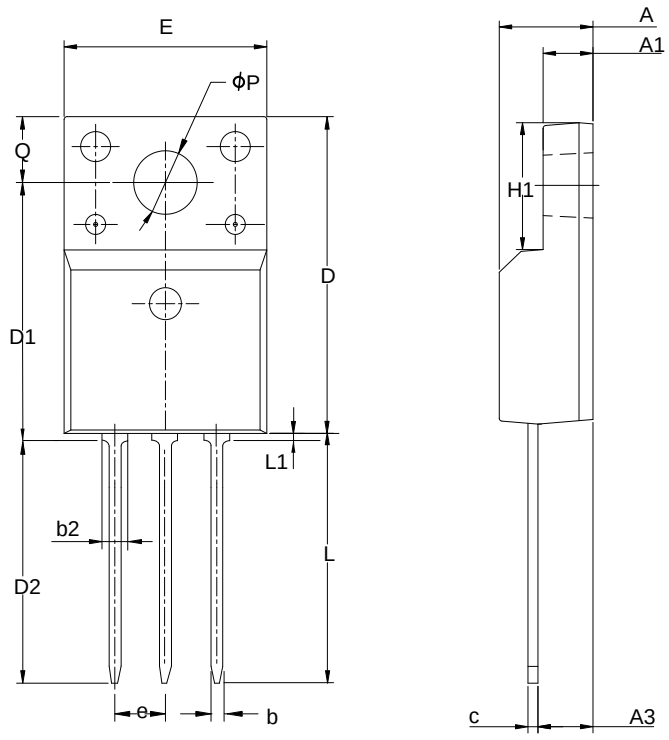


NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

PACKAGE OUTLINE(CONTINUED)

TO-220FJH-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.80
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	12.87	13.07	13.27
D2	12.28	12.48	12.68
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	0.85
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice:

1. Silan reserves the right to make changes of this instruction without notice.
2. Customers should obtain the latest relevant information when purchasing and should verify whether such information is latest and complete. Please read this instruction and application manual and related materials carefully before using products, including the circuit operation precautions, etc.
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7. Please use and apply product in compliance with all applicable laws and regulations, including but not limited to trade control regulations etc. The product is civil electronic product, please do not use it in non-civil fields.
8. Product promotion is endless, our company will wholeheartedly provide customers with better products!
9. Website: http: //www.silan.com.cn

Part No.:	SVS5N65F(D)(FJH)D2	Document Type:	Datasheet
Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http: //www.silan.com.cn

Rev.: 1.3

Revision History:

1. Update typical test circuit and package outline
2. Delete nomenclature
3. Update important notice
4. Update curve template

Rev.: 1.2

Revision History:

1. Add the package outline of TO-220FJH-3L

Rev.: 1.1

Revision History:

1. Add the package outline of TO-252-2L

Rev.: 1.0

Revision History:

1. First release